# Maintenance manual

# 9918 & 9921
# UHF Frequency Meter

RACAL
The Electronics Group

**Racal Instruments Limited** Duke Street, Windsor, Berks, England
Prepared by Central Handbooks Department, Racal Group Services Limited.

Printed in England Ref. WOH 8006 Issue 2.4.78-75

RACAL
WOH 8003

# UHF Frequency Meter 9921

Page

| | | Page |
|---|---|---|
| | Sampling Mixer Principles | 3-5 |
| | 'C' Channel Frequency Division | 3-6 |
| | Low Input Inhibit | 3-3 |
| | Sweep Speed-Up Circuit | 3-3 |
| | Compensator Circuit | 3-9 |
| CHAPTER 4 | TECHNICAL DESCRIPTION | |
| | INTRODUCTION | 4-1 |
| | LOGIC CIRCUIT SYMBOLS | 4-1 |
| | OFF-CHIP COUNTING DECADES | 4-2 |
| | 'A' CHANNEL INPUT | 4-2 |
| | Signal Input | 4-2 |
| | 'A' Channel Amplifier | 4-2 |
| | Threshold Detector | 4-2 |
| | $10^{o}$ Decade Inhibit | 4-3 |
| | Schmitt Trigger and 'A' Output | 4-3 |
| | Channel 'A' Inhibit | 4-4 |
| | Channels 'A', 'C' and Check Counting Path | 4-4 |
| | 'B' CHANNEL INPUT | |
| | Introduction | 4-4 |
| | Signal Path | 4-4 |
| | 'B' Channel Overload Protection | 4-4 |
| | P.I.N. Diode Attenuator | 4-5 |
| | Counter Inhibit Circuit | 4-6 |
| | Automatic Gain Control | 4-6 |
| | $10^{o}$ DECADE OUTPUTS | 4-6 |
| | $10^{o}$ and $10^{i}$ Decade Data Transfer | 4-6 |
| | Data Multiplexing | 4-6 |
| | SIGNAL INPUT TO CDI CHIP | 4-7 |
| | OVERFLOW DETECTOR | 4-7 |
| | DECIMAL POINT ENCODING | 4-7 |
| | CHECK LF AND 'C' CHANNEL SIGNAL GATING | 4-7 |
| | TIME BASE (GATE TIME) SELECTION | 4-8 |
| | CONTROL AND UPDATE | 4-8 |
| | Main Gate Output | 4-8 |
| | Data Transfer and Off-Chip Reset | 4-9 |
| | Display Time Generator | 4-9 |
| | Automatic Reset | 4-9 |
| | Manual Reset | 4-10 |
| | DATA OUTPUT AND DISPLAY SYSTEM | 4-10 |
| | Display | 4-10 |

| | | Page |
|---|---|---|
| | Sampling Mixer Principles | 3-5 |
| | 'C' Channel Frequency Division | 3-6 |
| | Low Input Inhibit | 3-3 |
| | Sweep Speed-Up Circuit | 3-3 |
| | Compensator Circuit | 3-9 |
| CHAPTER 4 | TECHNICAL DESCRIPTION | |
| | INTRODUCTION | 4-1 |
| | LOGIC CIRCUIT SYMBOLS | 4-1 |
| | OFF-CHIP COUNTING DECADES | 4-2 |
| | 'A' CHANNEL INPUT | 4-2 |
| | Signal Input | 4-2 |
| | 'A' Channel Amplifier | 4-2 |
| | Threshold Detector | 4-2 |
| | $10^{o}$ Decade Inhibit | 4-3 |
| | Schmitt Trigger and 'A' Output | 4-3 |
| | Channel 'A' Inhibit | 4-4 |
| | Channels 'A', 'C' and Check Counting Path | 4-4 |
| | 'B' CHANNEL INPUT | |
| | Introduction | 4-4 |
| | Signal Path | 4-4 |
| | 'B' Channel Overload Protection | 4-4 |
| | P.I.N. Diode Attenuator | 4-5 |
| | Counter Inhibit Circuit | 4-6 |
| | Automatic Gain Control | 4-6 |
| | $10^{o}$ DECADE OUTPUTS | 4-6 |
| | $10^{o}$ and $10^{i}$ Decade Data Transfer | 4-6 |
| | Data Multiplexing | 4-6 |
| | SIGNAL INPUT TO CDI CHIP | 4-7 |
| | OVERFLOW DETECTOR | 4-7 |
| | DECIMAL POINT ENCODING | 4-7 |
| | CHECK LF AND 'C' CHANNEL SIGNAL GATING | 4-7 |
| | TIME BASE (GATE TIME) SELECTION | 4-8 |
| | CONTROL AND UPDATE | 4-8 |
| | Main Gate Output | 4-8 |
| | Data Transfer and Off-Chip Reset | 4-9 |
| | Display Time Generator | 4-9 |
| | Automatic Reset | 4-9 |
| | Manual Reset | 4-10 |
| | DATA OUTPUT AND DISPLAY SYSTEM | 4-10 |
| | Display | 4-10 |

| | Page |
|---|---|
| Multiplex System | 4-11 |
| Display Drivers | 4-11 |
| LED INDICATORS | 4-11 |
| Overflow/Standby Indicator | 4-11 |
| MHz and Hz Indicators | 4-11 |
| Gate Indicator | 4-12 |
| External Standard Indicator | 4-12 |
| Overload Indicator | 4-12 |
| FREQUENCY STANDARD INPUTS | 4-12 |
| Frequencies | 4-12 |
| Internal Frequency Standard | 4-12 |
| Automatic Changeover | 4-12 |
| External Standard Input | 4-12 |
| Internal Standard Output | 4-13 |
| 500kHz Frequency Standard | 4-13 |
| FREQUENCY STANDARD OPTIONS | 4-13 |
| POWER SUPPLY | 4-13 |
| AC Supply | 4-13 |
| +5V Supplies | 4-13 |
| Standby | 4-14 |
| -5.2V and -10V Supplies | 4-15 |
| +24V Supply | 4-15 |
| CDI Chip +2V Supply | 4-15 |
| LF MULTIPLIER OPERATION (OPTION) | 4-15 |
| Signal Path | 4-15 |
| LF MULTIPLIER ASSEMBLY | 4-15 |
| Principle | 4-15 |
| Circuit Description | 4-16 |
| CIRCUIT DESCRIPTIONS 3GHz SECTION (9921) | 4-17 |
| TOP LOOP AND SAMPLER ASSEMBLY | 4-17 |
| Introduction | |
| Pulse Generator and Sampling Mixer | 4-17 |
| Output Buffer Amplifier for SM1 | 4-17 |
| Sampling Mixer No. 2 | 4-18 |
| Output Buffer Amplifier for SM2 | 4-18 |
| Top Loop Oscillator, Loop Filter and Sweep | 4-18 |
| Loop Filter and Sweep Circuit | 4-18 |
| Function of Q13 | 4-19 |
| Functions of Q11 | 4-19 |
| Voltage Controlled Oscillator (VCO 1) | 4-19 |

| | | Page |
|---|---|---|
| | Sweep Speed-Up Circuit | 4-20 |
| | DIGITAL OFFSET COMPENSATOR ASSEMBLY | 4-20 |
| | Introduction | 4-20 |
| | Circuit Description | 4-21 |
| | 2nd LOOP AND OUTPUT PROCESSOR ASSEMBLY 19-0357 | 4-21 |
| | 2nd Loop Oscillator and Division System | 4-22 |
| | Output Processor Circuits | 4-22 |
| | AGC | 4-23 |
| | Frequency Doubler | 4-23 |
| | Low Level Detection and Inhibit | 4-23 |
| CHAPTER 5 | MAINTENANCE | |
| | INTRODUCTION | 5-1 |
| | LIST OF TEST EQUIPMENT REQUIRED | 5-1 |
| | REMOVAL OF COVERS | 5-2 |
| | POWER SUPPLY PREPARATION | 5-3 |
| | Power Lead | 5-3 |
| | Supply Fuse | 5-3 |
| | AC (Mains) Voltage Selection: General | 5-3 |
| | AC (Mains) Voltage Selection (Earlier Models) | 5-3 |
| | AC (Mains) Voltage Selection (Later Models) | 5-4 |
| | POWER CIRCUIT RESISTANCE CHECK | 5-4 |
| | POWER SUPPLY VOLTAGE CHECKS | 5-6 |
| | SELF CHECK | 5-7 |
| | SENSITIVITY AND AGC CHECK: INPUT 'A' | 5-8 |
| | SENSITIVITY AND AGC CHECK: INPUT 'B' | 5-9 |
| | OFF-CHIP COUNTER CHECK | 5-11 |
| | FREQUENCY STANDARD CHECKS | 5-11 |
| | Frequency Standard Input/Output Check | 5-12 |
| | Internal Frequency Standard Calibration | 5-12 |
| | CALIBRATION: INPUT 'C' (9921 ONLY) | 5-13 |
| | SUPPLEMENTARY CALIBRATION PROCEDURES (9921) | 5-14 |
| | INTRODUCTION | 5-14 |
| | TOP LOOP AND SAMPLER ASSEMBLY | 5-14 |
| | Test Equipment | 5-14 |
| | Power Check | 5-14 |
| | Disconnections | 5-15 |
| | VCO Setting-Up Procedure | 5-15 |
| | Filter Check | 5-15 |
| | Dual Sampler Check | 5-17 |
| | Sweep Speed-Up Circuit | 5-18 |

Page

2nd LOOP AND OUTPUT PROCESSOR ASSEMBLY 19-0857 5-20

Preliminary 5-20
Test Equipment 5-20
Power Check 5-20
Phase Locked Loop 5-20
Output Processor Check 5-21

CHAPTER 6 DISMANTLING AND REASSEMBLY

INTRODUCTION
REMOVAL OF MAIN PCB
REMOVAL OF DISPLAY ASSEMBLY
3GHz SECTION ASSEMBLIES
REMOVAL OF FREQUENCY STANDARD
FITTING REMOTE CONTROL AND BCD OUTPUT ASSEMBLY
FITTING LF MULTIPLIER ASSEMBLY (OPTION 09)

IN TEXT ILLUSTRATIONS

Fig. No.

| | | |
|---|---|---|
| 2.1 | Front Panel 9921 | 2-3 |
| 3.1 | Simplified Block Diagram | 3-1 |
| 3.2 | Multiplex Display System | 3-3 |
| 3.3 | D.I.L. Resistor Array | 3-4 |
| 3.4 | Sampling Mixer Principles | 3-6 |
| 3.5 | 'C' Channel Frequency Division | 3-7 |
| 4.1 | 'A' Channel Output | 4-3 |
| 4.2 | Theoretical P.I.N. Diode Attenuator | 4-5 |
| 4.3 | +5V Switching in Standby Mode | 4-14 |
| 5.1 | Voltage Selector (Later Models) | 5-5 |
| 5.2 | Sweep Waveform Diagram | 5-13 |
| 5.3 | Sweep Speed-Up and Lock | 5-16 |
| 5.4 | Sampler Sub-Assembly Test Points | 5-17 |
| 5.5 | Sweep Test Switch | 5-19 |
| 5.6 | Terminating Network | 5-21 |

## LIST OF TABLES


| Tables | | Page |
|---|---|---|
| 1 | Remote Input Selection | Tech. Spec. (7) |
| 2 | Time Base Program | Tech. Spec. (7) |
| 3 | Remote Control Connector: Pin Functions | Tech. Spec. (8) |
| 4 | 50-Way Data Output Socket | Tech. Spec. (10) |
| 5a & 5b | FM Tolerance | Tech. Spec. (11) |
| 6 | List of Test Equipment | 5-1 |
| 7 | Mains Voltage Selection Switches (Early Models) | 5-4 |
| 8 | Power (Mains) Input Circuit Resistance | 5-5 |
| 9 | 9921: Pin 14 Voltage/Resistor Values | 5-6 |
| 10 | Self Check Display | 5-7 |
| 11 | Self Check in LF Mode (Option) | 5-8 |
| 12 | 'A' Channel Sensitivity | 5-9 |
| 13 | Sensitivity Check: Input 'B' | 5-10 |
| 14 | Filter Response Check: 19-0356 | 5-17 |
| 15 | LF Multiplier Connections (Option 09) | 6-4 |

SECTION 3 PARTS LIST, COMPONENT LAYOUTS AND CIRCUIT DIAGRAMS

Refer to the Contents List at the beginning of Section 3.

SECTION 4 APPENDICES AND CHANGE INFORMATION

# SECTION 1

# TECHNICAL SPECIFICATION

# TECHNICAL SPECIFICATION

NOTE: The following information applies to both the 9918 and 9921 except that the 'C' channel is not fitted to the 9918.

## DISPLAY

| | |
|---|---|
| Format: | Nine, 7 segment LED's. Decimal point positioned automatically. |
| Latch: | Previous measurement is displayed during period required to complete new measurement. Display is updated automatically at end of each measurement. |
| Display Time: | Approximately equal to gate time plus 30ms. |
| Reset: | Manual or automatic. |
| Check: | With Check/Operate/Reset Switch in Check position display reads as follows, according to INPUT switch position.<br>INPUTS A and C - counter reads 1MHz to check operation.<br>INPUT B - all digits set to 8 to check all segments. |
| Range Indicators: | Two LED's indicate Hz and MHz respectively. |
| Gate Indicator: | LED illuminated when main gate is open. |
| Overflow/Standby/Indicator: | LED illuminates:-<br>(a) When display overflows<br>or<br>(b) When the INPUT switch is set to REMOTE (with the Remote Option not fitted). This indicates that the frequency standard remains in operation.<br>or<br>(c) When Remote Option is fitted and programmed to Standby. |
| External Standard Indicator: | LED indicates when external standard is in use. |

## INPUT A

| | |
|---|---|
| Frequency Range: | 10Hz - 100MHz HF<br>10Hz - 5kHz LF Multiplier Option. |
| Sensitivity: | Better than 10mV r.m.s. up to 70MHz<br>Better than 50mV r.m.s. at 100MHz. |
| Input Impedance: | 1MΩ in parallel with 25pF. |
| Maximum Input Levels: | 250 r.m.s. up to 100kHz decreasing to 10V r.m.s. above 10MHz. 400V d.c. |
| AGC: | AGC is effective over a wide dynamic range and a clipping circuit becomes effective above 10V peak to peak. |

## INPUT B

| | |
|---|---|
| Frequency Range: | 40MHz to 560MHz |
| Sensitivity: | Better than 10mV r.m.s. |
| Signal Range: | 10mV to 5V r.m.s. with automatic gain control. |
| Input Impedance: | 50Ω nominal. |
| Overload Protection: | Up to 35V r.m.s. maximum by pin diode attenuator and reed relay. |
| Overload Indicator: | LED illuminates when level exceeds approximately 5V. |
| AGC: | 50dB minimum range. |

## INPUT C (9921 only)

| | |
|---|---|
| Frequency Range: | 300MHz to 3GHz. |
| Sensitivity: | Better than 50mV r.m.s. |
| Signal Range: | 50mV to 1V r.m.s. |
| Input Impedance: | 50Ω nominal. |
| Maximum Input Levels: | a.c., 2.25V r.m.s.<br>d.c., d.c. plus peak a.c. not to exceed 100V. |
| Operating Temperature Range: | 0 to 50°C. |

## FREQUENCY MEASUREMENT

| | |
|---|---|
| Range: | 9918: 10Hz to 560MHz (Inputs A and B)<br>9921: 10Hz to 3GHz (Inputs A, B, and C). |
| Accuracy: | ± 1 count ± frequency standard accuracy. |
| Gate Times: | Inputs A and B: 0.01s, 0.1s, 1.0s and 10s.<br>Input C (9921): 0.02s, 0.2s, 2.0s and 20s. |
| Resolution: | Inputs A and B: 100Hz, 10Hz 1.0Hz and 0.1Hz.<br>Input C (9921): 10kHz, 1kHz, 100Hz and 10Hz. |
| LF Multiplier: | See Option 09. |

## FREQUENCY STANDARD 04A

| | |
|---|---|
| Type: | Model 9442. A fast warm-up ovened oscillator suitable for the vast majority of applications and normally fitted unless otherwise requested. |
| Frequency: | 5MHz. |
| Ageing Rate: | ± 3 parts in $10^9$/day after 3 months continuous operation. |
| Warm-up Time: | Better than ± 2 parts in $10^7$ within 6 minutes. |
| Temperature Stability: | Better than ± 3 parts in $10^9$ per °C over the range -10°C to +45°C. |

## FREQUENCY STANDARD 04B

| | |
|---|---|
| Type: | Model 9421. An ovened oscillator of the utmost precision for use when the highest long term accuracy is essential. |
| Frequency: | 5MHz. |
| Ageing Rate: | ± 5 parts in $10^{10}$/day after 3 months continuous operation. |
| Warm-up Time: | Better than ± 1 part in $10^7$ within 20 minutes. |
| Temperature Stability: | Better than ± 6 parts in $10^{10}$ per °C over the range -10°C to +45°C. |

## FREQUENCY STANDARD 04C

| | |
|---|---|
| Type: | An unovened crystal oscillator suitable for non-critical applications or where the instrument will normally be be used with the customer's external standard. |
| Frequency: | 5MHz. |
| Ageing Rate: | ± 1 part in $10^6$ per month. |
| Temperature: | ± 8 parts in $10^6$ over temperature range 0°C to +55°C.<br>± 3 parts in $10^6$ over temperature range +20°C to +40°C. |

## STANDARD FREQUENCY OUTPUT

| | |
|---|---|
| Frequency: | 1MHz. |
| Level: | Standard t.t.l. output. |
| Waveform: | Approximately rectangular. |
| Connector: | BNC socket on rear panel. |

## EXTERNAL STANDARD INPUT

| | |
|---|---|
| Frequency: | 1MHz |
| Minimum Level: | 500mV r.m.s. |
| Maximum Level: | 10V r.m.s. 400V d.c. |
| Input Impedance: | Approximately 200Ω(a.c. coupled). |
| Connector: | BNC socket on rear panel. The instrument automatically changes to external standard when standard input is connected. |

## POWER REQUIREMENTS

| | |
|---|---|
| Supply Voltage | 94-115V, 112-127V, 188-230V, 225-265V. Selected by rear panel switches. |
| Frequency: | 45-450Hz. |
| Consumption: | Approximately 24VA. |

## ENVIRONMENTAL CONDITIONS

| | |
|---|---|
| Specification: | Meets the majority of the requirements of REMC/20 FR Cat.3 Issue 6. |
| Operating Temperature : | -5°C to +55°C up to 560MHz operation.<br>0°C to +50°C for 3GHz operation. |
| Storage Temperature: | -40°C to +70°C. |

## MECHANICAL

| | |
|---|---|
| Dimensions: | Height 110 mm overall, 83 mm without feet.<br>Width 399 mm overall, 355.5 mm without handle.<br>Depth 298.5 mm. |
| Weight: | 3.75 kg (9921). 3.25kg (9918) Approx. |

## REMOTE-BCD OPTION KIT ASSEMBLY (Part No. 11-1242)

| | |
|---|---|
| BCD Data Outputs: | Provides display data output in parallel forms; 4 line BCD weighted 1248 per display digit, 3 line decimal point position, single line units information and over-flow. Command output 1 ms pulse. Input information, Hold/Reset and Print Hold. TTL output levels. |
| Remote Control: | Selected by front panel switch.<br>Provides control of time base programme (3 line binary coded) channel selection (2 lines) standby selection (1 line). Input logic levels '0' state -12V to +0.4V, '1' state +2.4V to +12V. |

## OPTION 04 : ALTERNATIVE FREQUENCY STANDARDS

Refer to pages Tech.Spec (3) and (4).

## OPTION 09 LF MULTIPLIER

| | |
|---|---|
| Function: | To increase measurement resolution at low frequencies on 'A' Input Channel. |
| Frequency Range: | 10Hz to 5kHz. |
| Resolution: | X 100 improvement in resolution. |
| Filtering: | Selected internally automatically. |

## ACCESSORIES PROVIDED

(1) Bag containing spare fuses.
(2) Operators Handbook.

## OPTIONAL ACCESSORIES

| | |
|---|---|
| Rack Mounting Kit: | Part No. 11-1006. |
| Solid Carrying Case: | Part No. 15-0450. |
| Padded Carrying Case: | Part No. 15-0478. |

# SUPPLEMENTARY DATA

## REMOTE-BCD OPTION 02 : REMOTE CONTROL DETAILS

Connector:

14-way Type 57 accessible on rear panel. For pin functions refer to page Tech.Spec. (8) Table 3.

Input Selection:

Two control lines (J and K) coded as follows:-

TABLE 1

Remote Input Selection

| Input Channel | Control Logic J | K |
|---|---|---|
| A (LF)* | 1 | 1 |
| A (HF) | 0 | 1 |
| B | 1 | 0 |
| C | 0 | 0 |

* When LF Option fitted.

Time Base Program:

Three binary coded lines (x, y and z) as follows:-

TABLE 2

Time Base Program

| Inputs A & B Gate Times | Input C Gate Times (9921 only) | Control Logic x | y | z |
|---|---|---|---|---|
| .01 | .02 | 1 | 0 | 0 |
| .1 | .2 | 0 | 1 | 0 |
| 1s | 2s | 1 | 1 | 0 |
| 10s | 20s | 0 | 0 | 1 |

REMOTE-BCD OPTION 02 : REMOTE CONTROL (Continued)

Operate/Standby Select: A single control line (Table 3 pin 9) switches the instrument d.c. power supply, as follows:-

Logic '1' Standby: power is off except to internal frequency standard.

Logic '0' Operate: instrument is fully operational.

External Remote Select: Logic level on pin 12 (Table 3) selects remote control from external source , as follows:

Logic '1'--- selects remote control.

Logic '0' (or open circuit) reverts to local control.

Hold Input: Table 3 pin 11: '1' level holds the counter after the completion of the gate time in progress.

Hold/Reset Input: Table 3 pin 10: '1' level holds the counter. The transition from '1' to '0' level initiates counter reset.

DC Supply: Table 3 pin 2: +5V (nominal) output via 180Ω.

Logic Level Range: '0' state: -12V to +0.4V.
'1' state: +2.4V to +12V.

Table 3: Remote Control Connector : Pin Functions

| Pin No. | Function | |
|---|---|---|
| 1 | Not Used | |
| 2 | + 5V output line via 180Ω | |
| 3 | Timebase program z line ) | Refer to Table 2 |
| 4 | Timebase program y line ) | |
| 5 | Timebase program x line ) | |
| 6 | 0V. Output line | |
| 7 | Input select, J line ) | Refer to Table 1 |
| 8 | Input select, K line ) | |
| 9 | Operate/Standby select input line | |
| 10 | Hold/Reset input line | |
| 11 | Hold input line | |
| 12 | External Remote Select | |
| 13 | Not Used | |
| 14 | Not Used | |

## REMOTE - BCD OPTION KIT: DATA OUTPUT DETAILS

### BCD OUTPUT

| | |
|---|---|
| Display Information Format: | 9 digit 4 line BCD (weighted 1, 2, 4, 8 per display digit) and 3 line decimal point position. |
| Units: | Single line: MHz '1' level<br>Hz '0' level |
| Overflow: | Single line: overflow is indicated by a '1' level. |
| Command Output: | A positive going pulse of 1ms duration is provided. |
| Print Hold Input: | A '1' level holds the counter after completion of a gate time. |
| Hold/Reset Input: | A '1' level hold the counter. The transition from '1' level to '0' level initiates reset. |
| BCD Output Logic Levels: | '0' state 0V to + 0.4V<br>'1' state +2.4V to +5V<br>Fan out, two standard TTL Loads. |
| BCD Control Input | '0' state, -12V to + 0.4V<br>'1' state, +2.4V to + 12V |

TABLE 4

50-Way Data Output Socket

| Digit | BCD | Pin No. | Digit | BCD | Pin No. |
|---|---|---|---|---|---|
| $10^0$ | 1 | 1 | $10^6$ | 1 | 13 |
| | 2 | 2 | | 2 | 14 |
| | 4 | 3 | | 4 | 15 |
| | 8 | 4 | | 8 | 16 |
| $10^1$ | 1 | 26 | $10^7$ | 1 | 38 |
| | 2 | 27 | | 2 | 39 |
| | 4 | 28 | | 4 | 40 |
| | 8 | 29 | | 8 | 41 |
| $10^2$ | 1 | 5 | $10^8$ | 1 | 18 |
| | 2 | 6 | | 2 | 20 |
| | 4 | 7 | | 4 | 42 |
| | 8 | 8 | | 8 | 44 |
| $10^3$ | 1 | 30 | Decimal Point | 1 | 45 |
| | 2 | 31 | | 2 | 46 |
| | 4 | 32 | | 4 | 47 |
| | 8 | 33 | | | |
| $10^4$ | 1 | 9 | *Time Base x | | 21 |
| | 2 | 10 | *Time Base y | | 22 |
| | 4 | 11 | *Time Base z | | 23 |
| | 8 | 12 | 0V. | | 25 |
| $10^5$ | 1 | 34 | LF | | 43 |
| | 2 | 35 | +5V | | 50 |
| | 4 | 36 | OVERFLOW | | 17 |
| | 8 | 37 | PRINT COMMAND | | 48 |
| | | | PRINT HOLD | | 49 |
| | | | HOLD/RESET | | 24 |
| | | | Not used | | 19 |

* See Table 2.

# APPENDIX 1

## 9921 3GHz SECTION

### FM Tolerance

The tables below show the accuracy of readout when measuring frequency modulated signals at two different input levels. The accuracy is given as either ±5kHz or ±1 count, together with the maximum deviations for a selection of modulating frequencies.

TABLE 5a

FM Tolerance at 0dBm Input Level

| Carrier | 300MHz | | 1GHz | | 3GHz | |
|---|---|---|---|---|---|---|
| Accuracy | ±5kHz | ±1 count | ±5kHz | ±1 count | ±5kHz | ±1 count |
| Modulating Freq. | maximum deviations | | | | | |
| 50Hz | 60kHz | 10kHz | 150kHz | 30kHz | 300kHz | 90kHz |
| 100Hz | 30kHz | 5kHz | 75kHz | 15kHz | 150kHz | 45kHz |
| 200Hz | 15kHz | 2.5kHz | 36kHz | 7.5kHz | 75kHz | 22kHz |
| 500Hz | 6kHz | 1kHz | 15kHz | 3kHz | 30kHz | 9kHz |
| 1kHz-50kHz | 5kHz | 1kHz | 10kHz | 3kHz | 20kHz | 9kHz |

TABLE 5b

FM Tolerance at -13dBm Input Level

| Carrier | 300MHz | | 1GHz | | 3GHz | |
|---|---|---|---|---|---|---|
| Accuracy | ±5kHz | ±1 count | ±5kHz | ±1 count | ±5kHz | ±1 count |
| Modulating Freq. | maximum deviations | | | | | |
| 50Hz | 15kHz | 10kHz | 37kHz | 30kHz | 75kHz | 90kHz |
| 100Hz | 7.5kHz | 5kHz | 19kHz | 15kHz | 37kHz | 45kHz |
| 200Hz | 4kHz | 2.5kHz | 9kHz | 7.5kHz | 19kHz | 22kHz |
| 500Hz | 1.5kHz | 1kHz | 4kHz | 3kHz | 7kHz | 9kHz |
| 1kHz-50kHz | 1.2kHz | 1kHz | 2.5kHz | 3kHz | 5kHz | 9kHz |

# SECTION 2

# DESCRIPTION

# OPERATION & MAINTENANCE

# CHAPTER 1

# GENERAL DESCRIPTION

## INTRODUCTION

1.1 The 9918 and 9921 are similar nine-digit frequency meters which differ in frequency range. The 9918 is a two-channel instrument with a range of 10Hz to 560MHz; the 9921 has an additional 'C' channel which extends the coverage to 3GHz.

1.2 The instruments are designed around a CDI integrated circuit device of very high reliability which replaces the majority of the logic encountered in conventional digital frequency meters. This reduces size, weight, power consumption, temperature rise and cost, and at the same time ensures reliability and ease of maintenance.

## INPUTS

1.3 The input channels provided are as follows:-

INPUT 'A' The frequency range is 10Hz to 100MHz, directly gated, with automatic gain control. The input impedance is 1MΩ in parallel with 25pF and the sensitivity better than 10mV up to 70MHz and 50mV at 100MHz. An optional LF Multiplier assembly is available, which increases the resolution on this channel by a factor of 100 in the frequency range 10Hz to 5kHz. When this option is fitted an additional (HF/LF) switch is fitted on the front panel.

INPUT 'B' The frequency range is 40MHz to 560MHz, directly gated, with automatic gain control and overload protection. The input impedance is 50Ω and sensitivity better than 10mV.

INPUT 'C' (9921 only) The frequency range is 300MHz to 3GHz, prescaled by 200. The time base (gate time) is automatically doubled, and the decimal point positioned, to retain direct reading of the frequency display.
The input impedance is 50Ω and the sensitivity better than 50mV.

## DISPLAY

1.4 The nine-digit latched display uses seven-segment l.e.d. indicators with automatic positioning of the decimal point. Two l.e.d. indicators marked respectively 'Hz' and 'MHz' tell the user in which units to read the display. Other l.e.d. indicators are provided to show measurement in progress, external standard operation and display overflow/ standby. These are described in Chapter 2.

## FREQUENCY STANDARD

1.5 Customers are offered a choice of two high stability temperature controlled frequency standards from the Racal range, or an unovened oscillator. Details are given on pages Tech.Spec. (3) and (4). The high stability units should be serviced only by Racal Instruments, or authorised agents. An aperture in the rear panel provides access for calibration of the frequency standard. A 1MHz reference frequency, derived from the standard in use, is available from a BNC socket on the rear panel.

1.6 When an external frequency standard is fed into the rear panel socket the instrument automatically changes to external standard operation, and the front panel l.e.d. illuminates to show this.

## POWER SUPPLY

1.7 The instrument operates from 94-127V, 188-265V a.c. supplies, 45 to 440Hz. Mains voltage selection is by means of two rear panel switches which provide four possible voltage selections and can be locked to the chosen positions by a screwed plate, which allows the selected voltage range markings to be seen. *Refer to para.5-5.

## DATA and REMOTE CONTROL OPTION

1.8 This option is identified as the 'Remote-BCD Option Kit Assembly Part No.11-1242'. It incorporates a p.c.b. assembly fitted in the instrument and two rear panel connectors; a 14-way connector for remote control and a 50-way connector for parallel BCD and other data outputs. Facilities, logic details and pin functions are described on pages Tech. Spec (7) to (10).

## HANDBOOK NOTES

### Differences Between 9918 and 9921

1.9 The 9921 is effectively a 9918 with a 3GHz section added. The reader should bear in mind the following:-

(1) The 9918 is not fitted with a 'C' channel.

(2) The multiplex reference frequency is 10kHz in both instruments except on 9921 'C' channel, when it becomes 5kHz with doubled gate time.

* Later models may be fitted with a different type of switch as described in para. 5.7.

# CHAPTER 2

# OPERATING INSTRUCTIONS

## PRELIMINARY

2.1 Before using the instrument for the first time, or at a new location, check the power supply as described in paras 5.3 to 5.7. The description of controls in this Chapter will assist the user in correct use of the instrument.

## INITIAL SETTINGS (LOCAL CONTROL)

2.2 Set the power switch to POWER ON, and the INPUT switch to REMOTE for standby mode.

## FREQUENCY MEASUREMENT (HF and UHF)

2.3 (1) Set the controls as follows:-

(a) CHECK/OPERATE/RESET switch to OPERATE.

(b) INPUT switch to the desired channel.

(c) LF MULTIPLIER switch (if fitted) to the normal (down) position.

(2) Connect the external signal to the appropriate input socket 'A', 'B' ('C' 9921). The symbol ⚠ advises the user to consult the handbook for further details. Maximum input levels are as follows:-

Damage Overload Input Levels

| Input 'A' | Input 'B' | Input 'C' (9921) |
|---|---|---|
| 250V r.m.s. up to 100kHz decreasing to 10V r.m.s. above 10MHz. Maximum d.c. level, 400V. | 35V r.m.s. | 2.25V r.m.s. DC level plus peak a.c. must not exceed 100V. |

(3) Check that the GATE indicator is illuminated.

(4) Select the appropriate gate time to give the desired display. The resolutions obtainable on the different channels are as follows:-

Resolution: Inputs 'A' and 'B'

| Gate Time (seconds) | .01 | 0.1 | 1 | 10 |
|---|---|---|---|---|
| Resolution | 100Hz | 10Hz | 1Hz | 0.1Hz |

(Resolution: Input 'C' (9921)

| Gate Time (Seconds) | .02 | 0.2 | 2 | 20 |
|---|---|---|---|---|
| Resolution | 10kHz | 1kHz | 100Hz | 10Hz |

## FREQUENCY MEASUREMENT (LF OPTION)

2.4 (1) Set the LF MULTIPLIER switch 'up' and the INPUT switch to channel 'A'.

(2) Connect the external signal (up to 5kHz) to the 'A' input socket. Select the required gate time.

Resolution: LF Multiplier Option

| Gate Time (second) | .01 | 0.1 | 1 | 10 |
|---|---|---|---|---|
| Resolution | 1Hz | 0.1Hz | .01Hz | .001Hz |

## REMOTE PROGRAM OPERATION (OPTION)

2.5 (1) Check that the remote control system is connected to the rear panel 14-way connector. For details of control data refer to pages Tech. Spec. (8) to (10).

(2) Set the INPUT switch to REMOTE.

(3) Connect the required input signals to the instrument front panel sockets.

(4) Set the instrument power switch to POWER ON.

(5) Operate the remote program as required.

NOTE: With the Remote Option in use allfront panel control functions, except POWER ON/OFF, are transferred to the remote control system.

## DESCRIPTION OF CONTROLS

## INDICATORS AND CONNECTIONS

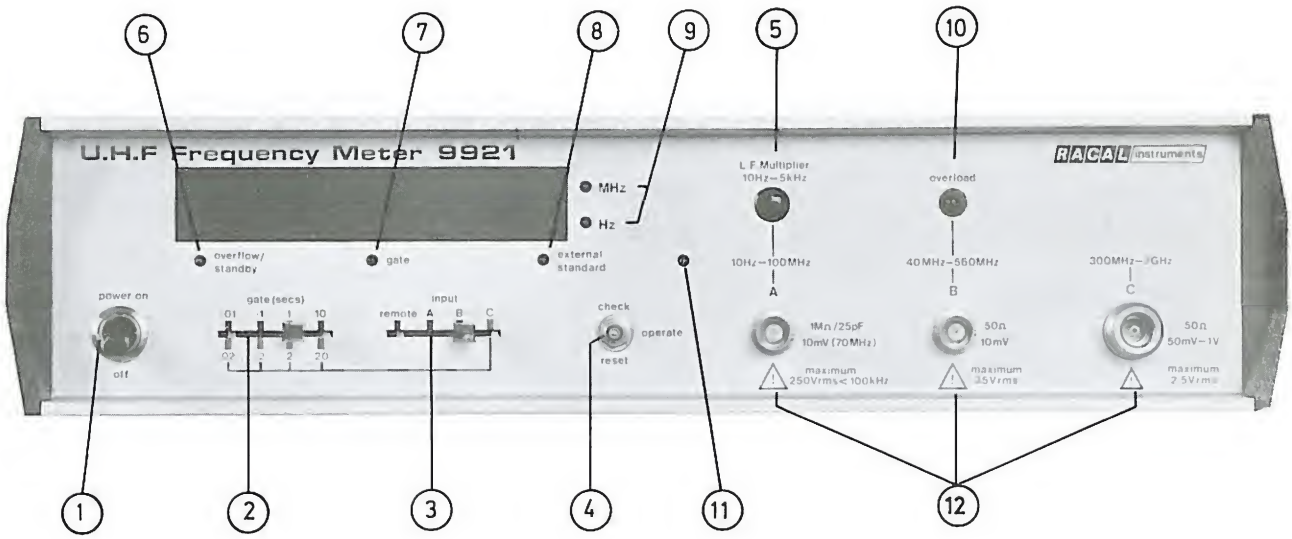
### CONTROLS

1 Power Switch:

This is a two-pole toggle ON/OFF switch which switches the a.c. supply to the voltage selection switches and main transformer.
In the OFF position all power is removed from the instrument circuitry. In the POWER ON position full power is provided and the display is illuminated.

Standby Facility*

In the POWER ON position a standby facility is available (provided the Remote Option is not fitted) by setting the INPUT switch to the REMOTE position. This cuts off the d.c. power to all circuits except the internal frequency standard and illuminates the OVERFLOW/STANDBY l.e.d. with display off.




**Front Panel : 9921 Fig. 2.1**

* When remote option is fitted the Standby facility is available by remote control.

| | | |
|---|---|---|
| 2 | GATE Switch: | The four positions select the appropriate gate time from the time base to give the required resolutions. The gate time markings above the switch refer to INPUTS 'A' and 'B', those below the switch refer to INPUT 'C' (9921). |
| 3 | INPUT Switch: | The positions 'A', 'B' and 'C' select the desired input channel. The REMOTE position selects remote programming when Option 02 is fitted. It also provides a standby facility (see Power Switch description). |
| 4 | CHECK/OPERATE/RESET Switch | In the CHECK position, with INPUT 'A' selected, the IMHz reference signal is fed through the counting and display circuits. With INPUT 'B' selected a segment check on the display is obtained.<br><br>OPERATE is the signal measurement mode.<br><br>When the RESET position is selected and released, the instrument will clear down to zero in readiness for a new measurement. |
| 5 | LF MULTIPLIER Switch: | This switch is fitted as part of the LF Multiplier option. It affects only the 'A' channel. When 'up' is selected the 'A' input is routed via the LF Multiplier option (maximum frequency 5kHz). For all normal measurements the 'down' position is used. |
| | INDICATORS | |
| 6 | OVERFLOW/STANDBY | This indicator illuminates when the measured frequency exceeds the capacity of a nine-digit display, showing that the most significant digit is being 'over-spilled'. It also functions as a standby indication (see Power Switch description on page 2-3). |
| 7 | GATE: | The GATE l.e.d. illuminates during the 'open' period of the main gate and goes off during the gate closed period, while the count is being displayed. Thus, during normal operation the l.e.d. 'blinks' in step with the successive measurements. In Hold mode the l.e.d. remains extinguished. |

8. EXTERNAL STANDARD — Illumination indicates that the instrument is operating from an external frequency standard.

9. MHz; Hz — Illumination indicates the units, of the frequency display. The 'Hz' indicator is operative only when LF Multiplier option is in use.

10. OVERLOAD — The overload l.e.d. illuminates when the 'B' input level exceeds approximately 5V r.m.s.

11. REMOTE — The l.e.d. illuminates when 'Remote' is selected. (Fitted from serial number 8235).

FRONT PANEL CONNECTIONS

12. INPUTS 'A", 'B' (and 'C' 9921 only). — These front panel sockets provide separate input connections for the different channels. The symbol ⚠ advises the user to consult the handbook for further details. The sockets 'A' and 'B' are BNC type; socket 'C' is type 'N'.

REAR PANEL ITEMS

Mains Voltage Selector: — This comprises two switches with either locking or cover plate. Refer to para.5.5.

Power Plug/Filter: — Contains a mains r.f. filter. A three-core power lead is supplied with the instrument.

Power Fuse: — A 5 x 20mm, glass cartridge, surge resisting type of fuse must be used. The fuse ratings are marked on the panel. The instrument is despatched with the 188V-260V fuse fitted. A spare fuse for 94V-130V use is supplied in the Accessories bag.

EXT STD I/P Socket: — BNC input socket for external frequency standard.

1MHz O/P Socket: — BNC. Provides 1MHz reference frequency from frequency standard in use.

Data Output/Remote Input connectors. — Details are given in Tables 3 and 4 on pages Tech.Spec. (8) and (10).

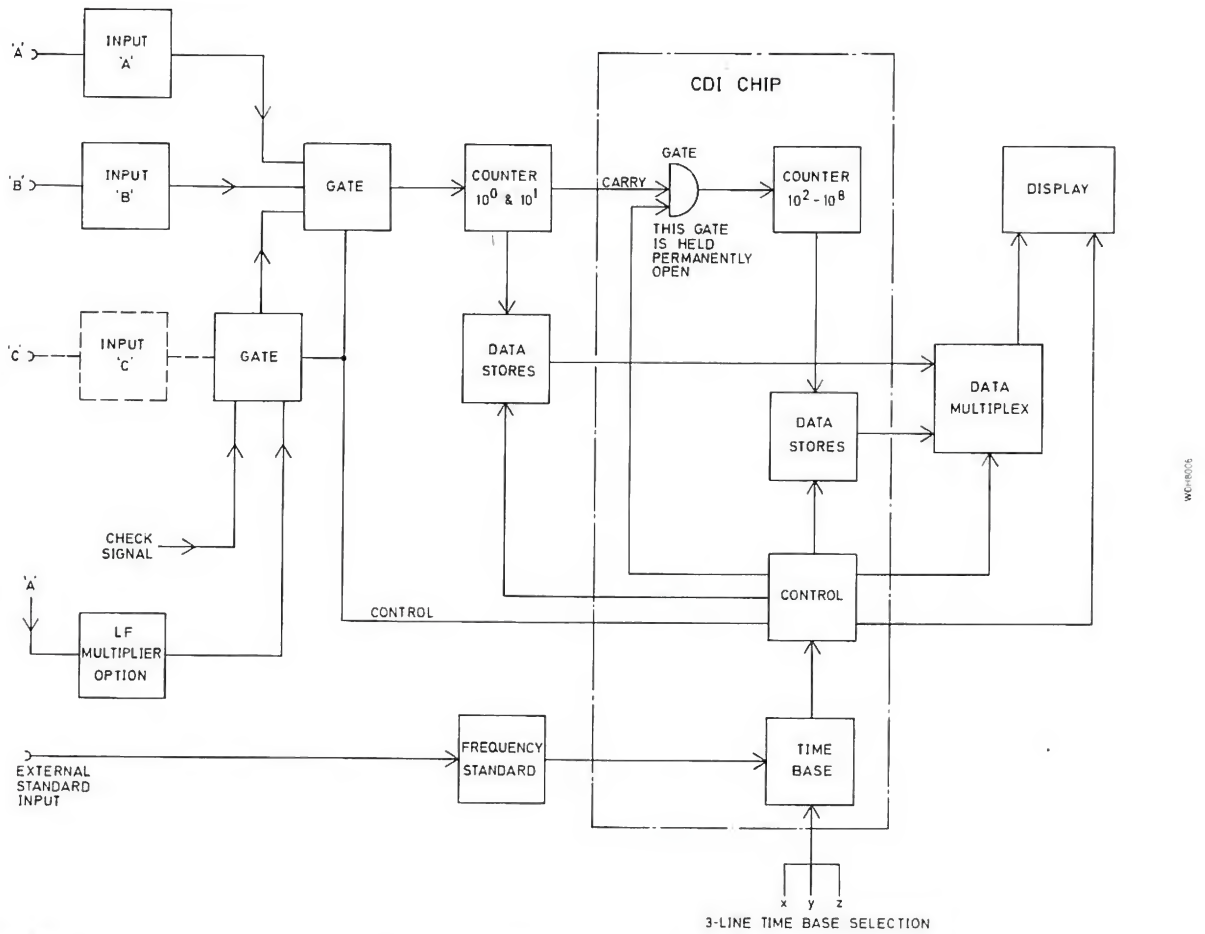
Osc. Adjust. — This aperture provides access to the frequency standard calibration adjustment.

# CHAPTER 3

# PRINCIPLES OF OPERATION

## BASIC FREQUENCY METER

3.1 A basic digital frequency meter comprises a chain of decade counters feeding b.c.d. data into latched stores. Counting is controlled via a main gate which is opened for a period determined by the time base. Provision is made for resetting the counter and releasing the data for display. In the 9918 and 9921 the majority of these functions are carried out in the CDI Chip (IC5 which achieves large scale integration (LSI), using the collector-diffusion-isolation process (CDI). Referring to Fig. 3.1, the input signal is gated first into the two off-chip decades which provide the readout data for the $10^0$ and $10^1$ digits. The 'carry' signal from the $10^1$ decade is fed into the counter in the CDI Chip, which provides the readout data for the $10^2$ to $10^8$ digits. The control system selects the required gating time from the time base, and arranges the correct release of data to the display. The multiplex output system and display is described in paras. 3.3 to 3.7. Input 'C' which is shown dotted, is fitted only in the 9921, and is described in paras. 3.10 to 3.25.




RACAL

Simplified Block Diagram Fig. 3-1

## GENERAL CIRCUIT FUNCTIONS

3.2 Outside the CDI Chip , other circuit functions are provided for, as follows:-

(a) Input amplification and signal shaping; automatic gain control and overload protection; input (channel) selection.

(b) A nine-digit display system in bit-parallel byte serial (multiplex) form, with data readout available for external use.

(c) Clock (reference) frequency generation using a high-stability temperature controlled oscillator, or an unovened oscillator, according to option.

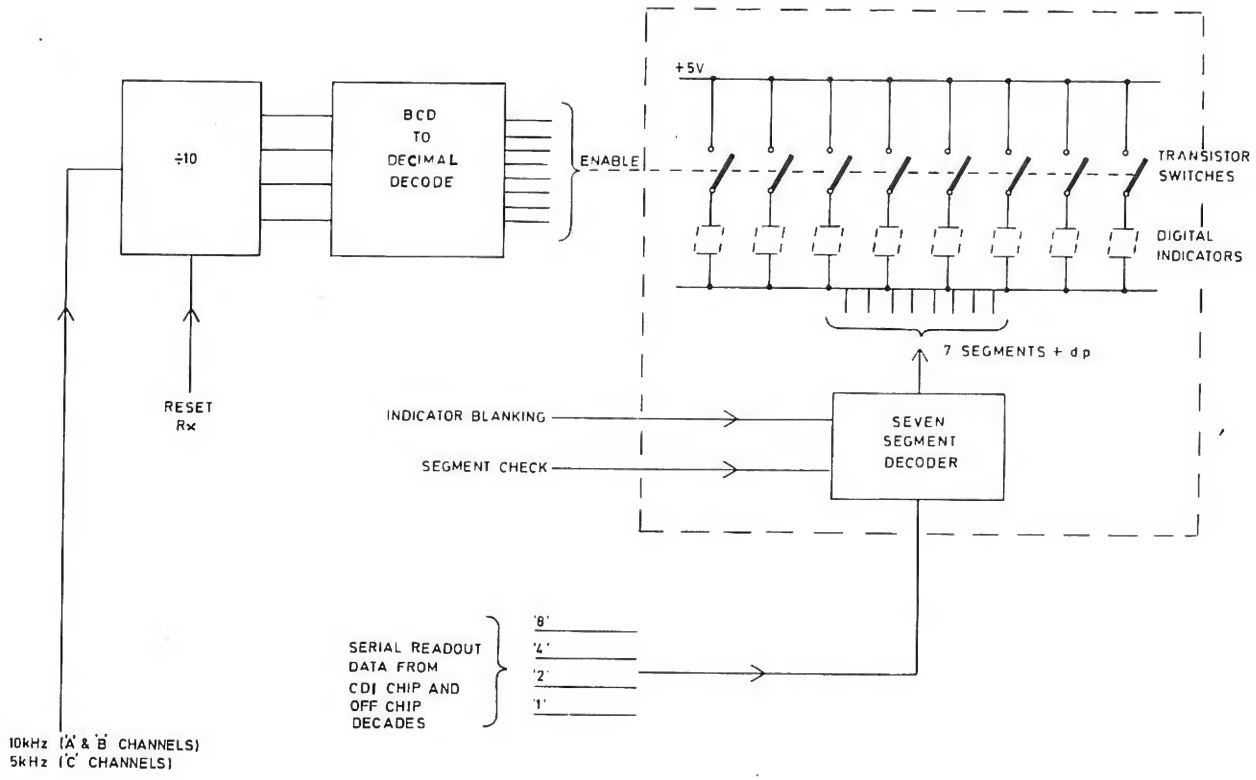
(d) The power supply system operates from a.c. mains and provides internal supplies of +5V, -5V, -10V, +24V and +2V.

(e) For the $10^0$ and $10^1$ information, off-chip counters, associated data stores and data multiplexing stages are provided.

(f) Light emitting diode (l.e.d.) indicators are provided to indicate operational conditions. (See Chapter 2).

## DYNAMIC DISPLAY SYSTEM

3.3 The Display Assembly contains a nine-digit display using light-emitting diodes as numerical indicators. These indicators are driven, via a multiplex stage and a 7 segment decoder, by the b.c.d. data output from the CDI Chip ($10^2$ to $10^8$) together with the multiplexed b.c.d. output from the two off-chip counter ($10^0$ and $10^1$). Each displayed numeral is formed by illuminating an appropriate number of short straight segments. The numeral '8', for example, is formed from 7 segments, where as numeral '5' will only require 5 segments.




Multiplex Display System Fig. 3.2

## Multiplex Display

3.4 The display data is fed from the data multiplex stage to the Display Assembly via a single four-wire b.c.d. connection. To permit this simple interconnection a parallel-to-serial (multiplex) system is used. This takes place on the CDI Chip, but the principles of de-multiplexing are shown in Fig. 3.2.

3.5 In the CDI Chip the data stores (digits $10^2$ to $10^8$) are gated into a b.c.d. four-line output, each store being enabled in sequence for 100µs. Similarly, the data stores for digits $10^0$ and $10^1$ feed in parallel a multiplex stage where the two four-line outputs are enabled in turn for approximately 100µs. The enabling signal is a 10kHz reference derived from the frequency standard when using channels 'A' and 'B', but 5kHz when channel 'C' (9921) is in use.

3.6 The multiplexed data from both the 'off chip' decades and the CDI Chip is fed to a 7 segment decoder (IC1) in the Display Assembly, which offers the decoded data to the bank of LED digital indicators. The 10kHz (5kHz on 'C' channel) reference signal is fed to a BCD Counter Decimal decoder which 'enables' each display LED in turn for 100µs. A reset pulse (Rx) which is generated during the $10^2$ state of the counter, ensures that the display enable is synchronised with the data store readout. Provision is made via IC1 for a segment check and also for automatically blanking out the display while the system is re-synchronising.

## Decimal Point

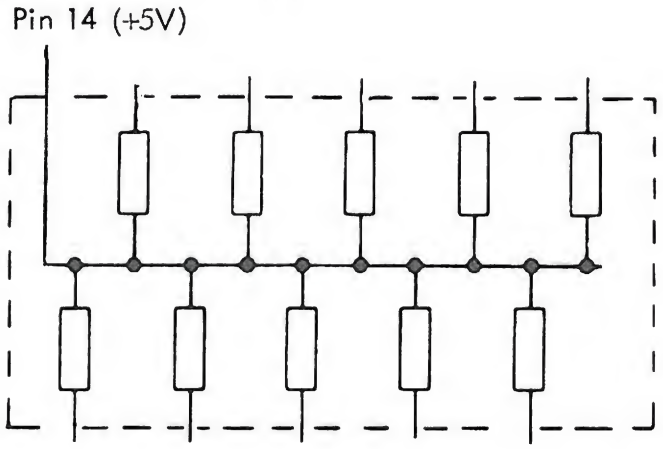
3.7 Decimal point (d.p.) illumination is obtained by encoding the time base control (GATE TIME) switch logic with the check/operate, A,B,C and LF channel control lines, in IC10. IC10 is a full adder, which adds the time base code to the b.c.d. number for the channel selected, or check mode. The output from IC10 feeds into a BCD-to-Decimal decoder on the display p.c.b. (IC2 in Fig.4).

## CONTROL CODES

3.8 A 3-line system is used for time base (gate time) selection. The lines are identified as x, y and z, and the logic coding is in Table 2 in the Technical Specification. Table 1 and Table 3 in the Technical Specification give details of the remote control system which is exercised via the rear panel 14-way socket SK1.

## RESISTOR ARRAYS

3.9 Many of the integrated circuits are 'open collector' types. For these IC's discrete 'pull-up' resistors are provided in the circuit. These resistors may be mounted in sealed dual-in-line (d.i.l.) packages, for example R100 (Fig.5) which has thirteen 10kΩ resistors with a common connection via pin 14 to +5V. Such arrays cannot be services and must be changed in the event of a faulty resistor. Figure 3.3 shows a 'pull-up' array schematically. Another type of resistor array comprises a d.i.l. package containing separate resistors of identical values, for example 1R1 in the Display Assembly (Fig.4) which contain eight 47Ω resistors.




D.I.L. Resistor Array Fig. 3.3

## FUNCTIONAL PRINCIPLES OF 3GHz SECTION (9921)

### Assemblies

3.10 The 'C' channel signals of the 9921 are processed in the 3GHz section which consists of three Assemblies, which are additional to the Main PCB and Display Assembly of the 9918. These are:-

(1) Top Loop and Sampler PCB 19-0856

(2) Sampler Sub-Assembly 19-0752

(3) 2nd Loop and Output Processor 19-0857

(4) Compensator PCB 19-0871

3.11 The output signal from the 3GHz section, which has been divided by 100, is fed into the main p.c.b. and gated into the frequency input of the CDI via the same path as the 'A' and 'B' signals.

### Theoretical Summary

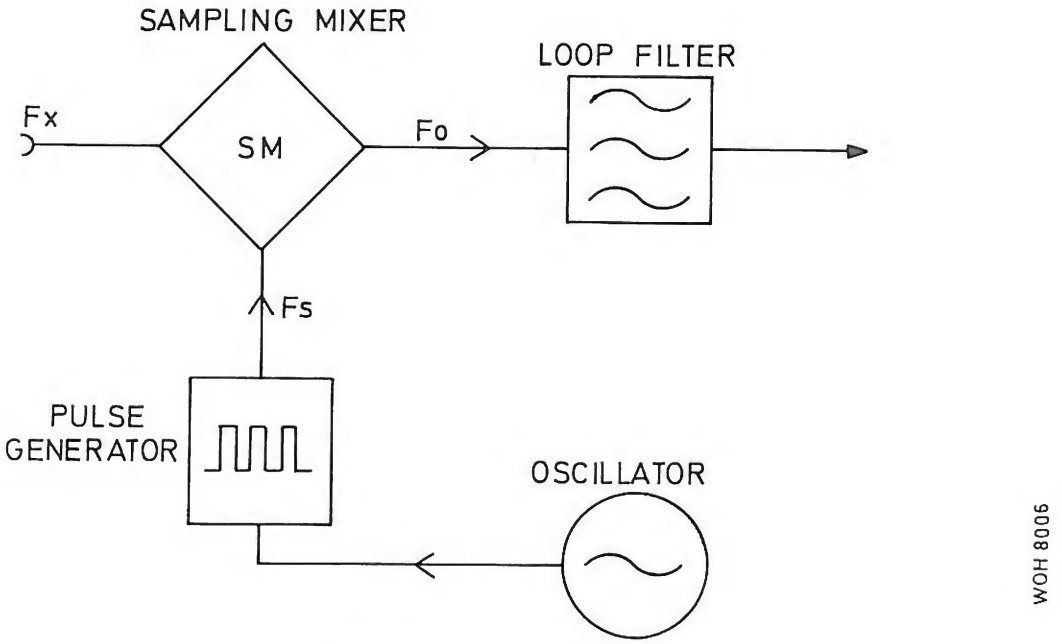
3.12 It is required that the 'C' channel signal be divided by 100 to operate within the range of the counter in the CDI Chip. The correct display being obtained by appropriate positioning of the decimal point. A simple digital division process is, however, not feasible with such ultra high-frequency signals. Therefore a technique using sampling mixers and phase-locked loops is employed, which produces division by 200. This signal is then fed to the counting decades, but the time base frequency (5MHz) used on 'C' channel is half that (10MHz) used on 'A' and 'B' channels, thus effectively producing an overall division by 100.

### Sampling Mixer Principles

3.13 A local oscillator signal is processed in a pulse generator to produce a train of narrow pulses of frequency $F_s$. The frequency spectrum of this pulse train is a comb of harmonically related "sampling" frequencies extending from $F_s$ to a very high frequency (determined by the width of the fundamental sampling pulse).

3.14 When an external signal, $F_x$, is applied to the sampling mixer SM it beats with each of the harmonics ($NF_s$) and produces numerous output beat frequencies, the lowest of which is selected by a low-pass filter. See Fig. 3.4

3.15 If the frequency $F_x$ is an exact harmonic of $F_s$ then the output $F_o$ will be a constant d.c. voltage. In all other cases the output frequency will be the difference between $F_x$ and the nearest harmonic of $F_s$.




Sampling Mixer Principles Fig.3.4

'C' Channel Frequency Division

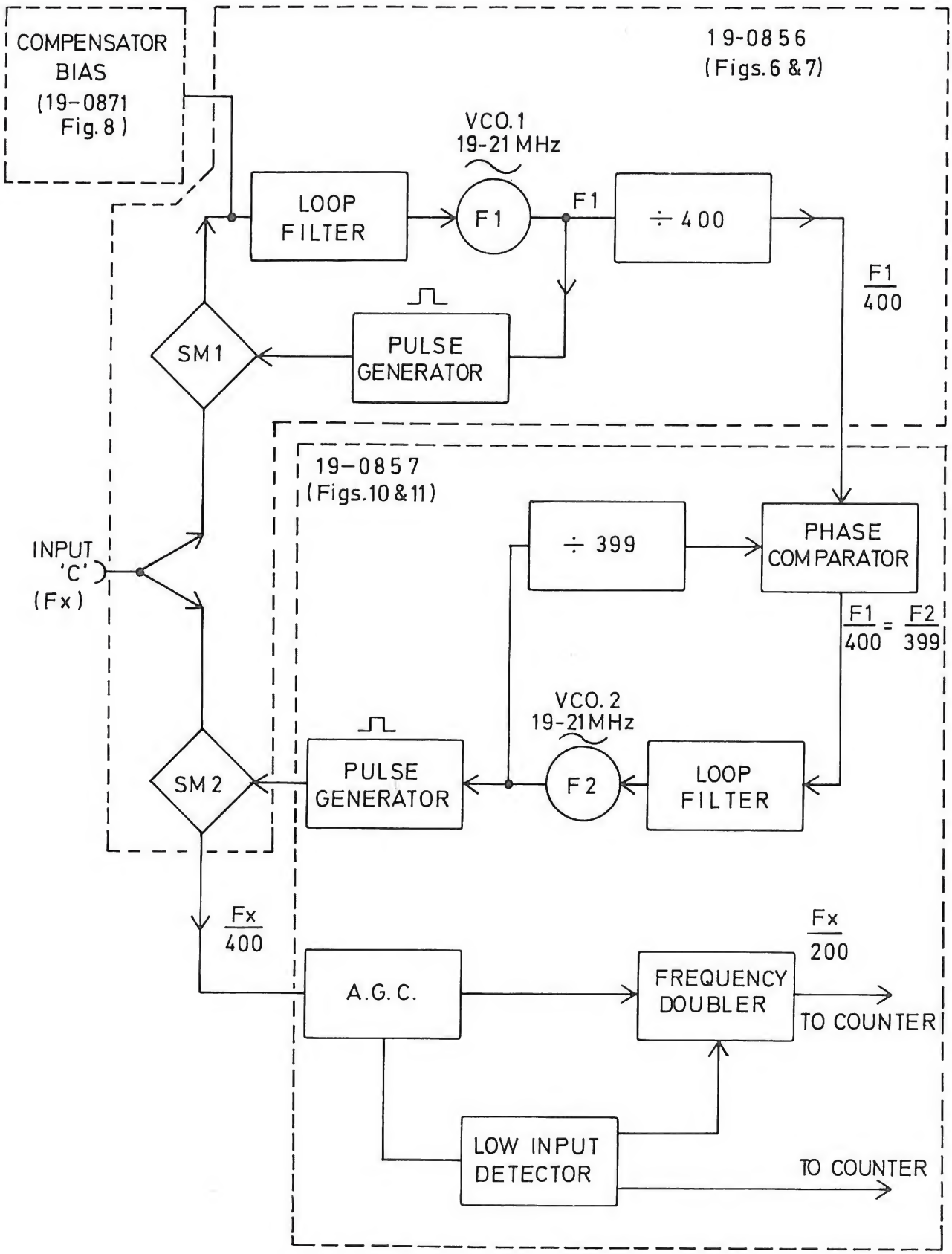
3.16 Referring to Fig. 3.5 the unknown input frequency $F_x$ is applied in parallel to two sampling mixers SM1 and SM2. Consider first top phase-locked loop comprising SM1 and the voltage controlled oscillator F1 (VCO 1), contained in p.c.b. 19-0856.

3.17 The VCO F1 drives a pulse generator which supplies narrow pulses to the sampling mixer SM1. When the loop is not locked the frequency of the VCO is swept continuously over the range 19-21MHz. When a harmonic of the sampling frequency (NF1) coincides with the external frequency $F_x$ the sweep stops and the d.c. signal now present at SM1 output holds the loop in lock. The Compensator board provides the correct bias to the Loop Filter to ensure correct operation over the designed temperature range.

3.18 After division by 400 in a digital divider the frequency F1/400 is applied to one input of a phase comparator.

3.19 The second loop comprises a VCO $F_2$, also operating in the 19-21MHz range. This oscillator signal $F_2$ is divided by 399 and then compared in frequency and phase with the signal F1/400. The output of the comparator pulls oscillator $F_2$ into lock such that:-

$$\frac{F_2}{399} = \frac{F_1}{400}$$




RACAL

WOH 8006

Channel 'C' Frequency Division

Fig. 3.5

$$F_2 = \frac{F_1 \times 399}{400}$$

Thus the frequency of oscillator $F_2$ is offset from oscillator $F_1$ by 1/400. This signal $F_2$ drives Sampling Mixer SM2 via a pulse generator.

3.20 The frequency ranges of oscillators $F_1$ and $F_2$ are restricted to ensure that the harmonic of $F_2$ which mixes with $F_x$ in Sampler SM2 will have the same harmonic number (N) as that used in SM1 and will therefore be offset from $F_x$ by 1/400. Thus a difference frequency will be produced in SM2 which is $F_x/400$.

3.21 This output $F_x/400$ is applied to the a.g.c. stage, and finally to a frequency doubler, before being fed to the combined main gate and $10^0$ counting decade in the main p.c.b.

3.22 The mathematics of the process may be summarized as follows:-

$$F_1 = \frac{F_x}{N}$$

or $NF_1 = F_x$

where $F_1$ = Freq. of VCO 1

$F_x$ = Unknown input freq.

N = harmonic number

$$\frac{F_2}{399} = \frac{F_1}{400}$$

where $F_2$ = Freq. of VCO2

thus:-

$$F_2 = \frac{399}{400} F_1$$

$$NF2 = \frac{NF_1 \times 399}{400} = \frac{F_x.399}{400}$$

$$F_x - NF_2 = \frac{F_x}{400}$$

Finally, Fx is doubled to give an output of $\frac{Fx.}{200}$

Low Input Inhibit

3.23 Precautions are taken against possible erratic counting arising from too low an input signal level. The low-level condition is detected in the Output Processor which applies an inhibit to the frequency doubler, thus producing an "all-zeros" display.

Sweep Speed-Up Circuit

3.24 A refinement not shown in Fig. 3.5 provides a higher sweep speed during part of

the oscillator tuning period, thus reducing the delay during the search for phase lock.

Compensator Circuit

3.25 This additional board is used to provide the correct bias to the Loop Filter in the top loop over the entire temperature range.

# CHAPTER 1

# TECHNICAL DESCRIPTION

## INTRODUCTION

4.1 The circuit description in this chapter apply to both the 9918 and 9921, except that any references to the 3GHz section ('C' channel) apply to the 9921 only. The description of the 9921 3GHz section commences at para. 4.94. It is assumed that the reader has a sound knowledge of solid state logic principles, and a clear understanding of the functional principles described in Chapter 3.

4.2 Apart from some switches and certain items of the power supply, the circuit for the basic instrument is mounted on one main p.c.b. assembly, with smaller assemblies for the display, reference oscillator, LF Multiplier Assembly option and 3GHz section. The part numbers and circuit diagrams are as follows:-

TABLE 5

LIST OF ASSEMBLIES

| Title | Assembly Reference | | Circuit Fig. No. |
|---|---|---|---|
| | 9918 | 9921 | |
| Main PCB (Motherboard) Assembly | 19-0855 | 19-0855 | Figs. 3 & 4 |
| Display Assembly | 19-0858 | 19-0858 | Fig. 4 |
| LF Multiplier Assembly (Option) | 19-0797 | 19-0797 | Fig. 13 |
| 5MHz Frequency Standard Oscillator | 9442 (or according to Option) | 9442 | |
| Remote and BCD Option Assembly | 19-0859 | 19-0859 | Fig. 14 |
| 9921 3GHz Section | | | |
| Top Loop and Sampler Assembly | - | 19-0856 | Figs. 6 & 7 |
| 2nd Loop and Processor Assembly | - | 19-0857 | Figs. 10 & 11 |
| Digital Offset Compensator Assembly | - | 19-0871 | Fig. 8 |

## LOGIC CIRCUIT REFERENCES

4.3 Extensive use is made of integrated circuits (IC's) and these are identified by a number and suffix letter. In the circuit description a particular IC pin will be identified by a reference such as 'IC10a/3', which indicates pin 3 on that particular gate. The logic symbols used in the circuits are those found in most manufacturers IC data sheets to which reference should be made if detailed information is required. The CDI Chip IC5 is, however, obtainable only through the Service Department of Racal Instruments Ltd.

## OFF-CHIP COUNTING DECADES

4.4 The counting chain for the $10^2$ -$10^8$ digit is contained within the CDI Chip IC5. There are, in addition, two 'off-chip' decades which are common to all channels; these are IC25 ($10^0$ decade) and IC6 ($10^1$ decade).

## 'A' CHANNEL INPUT

### Signal Input

4.5 Reference should be made to the circuit diagram Fig. 3. Signals in the range 10Hz to 100MHz are applied to the front panel 'A' input socket and fed to the amplifier via pins 29/30 on the Main PCB.

### 'A' Channel Amplifier

4.6 Referring to Fig. 3, the 'A' amplifier has a high impedance FET input (Q1) with overload protection by the clipping resistor R3, together with the gate-drain junction and diode D1. The output from Q1 source drives a wideband amplifier IC33, via emitter follower Q2 and the a.g.c. attenuator R7, R10, C4, C5, C6, D2 and D3.

4.7 From IC33 the signal passes via amplifier Q3. to emitter-follower Q4, which feeds the following circuits:-

(a) The threshold detector at IC31a/12.

(b) The Schmitt-Trigger at IC31b/9.

(c) The optional LF Multiplier p.c.b. 19-0797 via R24.

(d) The a.g.c. detector (D4, D5) and amplifier IC22.

### Threshold Detector

4.8 The purpose of the threshold detector is to inhibit measurement whenever the signal amplitude is too low for reliable counting. The circuit principle is that the threshold detector will inhibit the $10^0$ counting decade (IC25) until the input signal level is above the triggering threshold of the Schmitt Trigger IC31b.

4.9 IC31a will toggle when the input signal at IC31a/13 reaches 700-800mV, as compared with the triggering threshold of the Schmitt (IC31b) which is approximately 300-400mV. When IC31a toggles it charges C25, developing a voltage which enables IC21d and charges C26. When the voltage at IC22b/2 rises above the reference at IC22b/1, the output at IC22b/12 goes high, which, via D6, turns on Q10. The reference at IC22b/1 is the mid-point of the Vbb of IC31b.

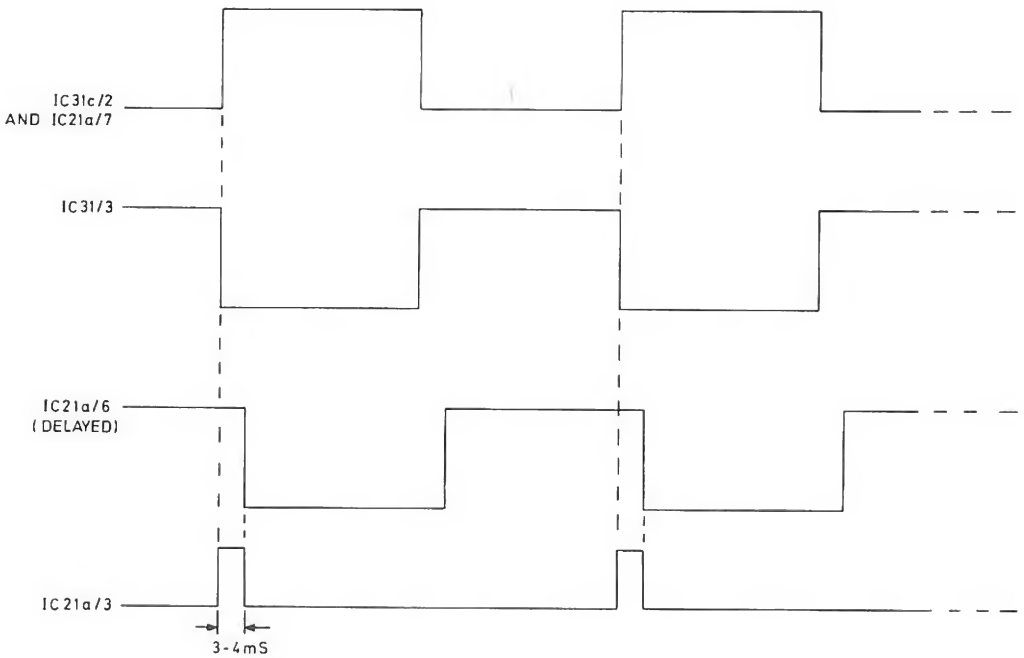
## $10^{o}$ Decade Inhibit

4.10 All the time that the signal level is too low for reliable counting Q10 remains 'off', and the OV number is applied to the reset input of IC20/4. This forces the $\overline{Q}$ of IC20 to the OV number, which inhibits the $10^{o}$ decade IC25. The inhibit is removed when the base of Q10 goes high, and this can be achieved via any of the 'wired-OR' inputs D6, D7, D8 or D9. The 'B' channel inhibit is described in para. 4.23.

## Schmitt Trigger and 'A' Output

4.11 IC31b is an ECL line receiver operating as a Schmitt Trigger, the shaped signal being fed to the amplifier IC31c which has two outputs, as follows.

4.12 The inverted output from IC21c/2 is fed direct to the gate IC21a/7 whereas the non-inverted output is fed via IC21c/10 and IC21b/4 to IC21a/6. These gates introduce a delay of approximately 4 nanoseconds and thus the gate IC21a is enabled for a period of approximately 4 nanoseconds in each cycle, giving an output pulse at IC21a/3 which is fed via Q6 to the $10^{o}$ counting decade. The waveforms are shown diagrammatically in Fig. 4.1.




'A' Channel Output Fig. 4.1

Channel 'A' Inhibit

4.13 When any channel other than 'A' is selected, a '0' is applied to IC21c/11 which disables IC21c and IC21a.

Channels 'A', 'C' and Check Counting Path

4.14 The base of Q6 is the common point in the 'A' channel, Check and 'C' channel (9921) signal paths. Q5 and Q6 form a convertor from the +5V ECL to -5V ECL, and Q34 is a clamp transistor to keep this ECL conversion within the correct limits.

4.15 From Q6 collector the selected signal is fed to the input of the $10^{o}$ decade at pin 16 of IC25. (Pin 16 on this IC can accept either the signal to be measured or an inhibit voltage). Counting will commence when the inhibit is removed, and this depends on the main gate waveform and the inhibit level at Q10 collector, both of which are applied via IC20. The 'Carry' output of IC25 is fed to the next ($10^{1}$) decade, which is IC6 in circuit diagram Fig. 4.

'B' CHANNEL INPUT

Introduction

4.16 The circuit is Fig. 3 at the back of the book. The 'Bp amplifier operates over the range 40MHz to 560MHz with 10mV sensitivity and has automatic gain control (a.g.c.) Overload protection is provided by a relay which interrupts the signal path should the input signal level rise above a pre-determined level. Power supplies of +5V, -5V and +24V are used.

Signal Path

4.17 The signal path will be described briefly, with more detailed descriptions commencing at para. 4.19. The signal is fed into the main p.c.b. at pin 23 thence via C34 and the contacts of the overload relay RLA to a p.i.n. diode attenuator (para. 4.21) and the input of the thick film amplifier IC30. Note that this amplifier has a +24V supply, which is turned on via Q35 and Q36, when the +5V 'B' supply is switched on by the INPUT switch S2a (Fig. 4).

4.18 From IC30 the signal is fed via a shunt feedback stage Q8 into parallel paths at C45 and C46. The signal via C46 feeds the a.g.c. detector D17 and D18 and is also used to enable the count. The signal at C45 is fed to the input of the common $10^{o}$ counting decade at IC25 pin 14.

'B' Channel Overload Protection

4.19 Although the fast acting a.g.c. system can cope with short term overloads, protection against longer term overload is provided by the protection circuit, which consists basically of the following items, with associated components:-

(a) Relay RLA, which is 'normally open' (i.e. the contact closes only when power is switched on.

(b) The diodes D9/D10 and capacitors C31/C35 which form a detector and voltage doubler.

(c) The operational amplifier IC32.

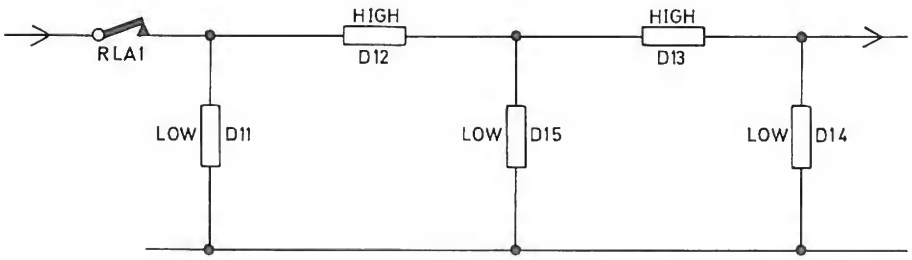
(d) Transistor Q7 which drives the front panel OVERLOAD indicator, LP50.

4.20 The input signal is fed via C31 to the detector D9/D10 and the rectified signal is applied to IC32. If the input signal rises above approximately 5V r.m.s., The output at IC32 will go high, which turns off relay RLA, thus interrupting the signal path. At the same time Q7 will turn on, causing the OVERLOAD l.e.d. to illuminate.

P.I.N. Diode Attenuator

4.21 The attenuator operates on the principle that the impedance of a diode varies according to the applied bias current. The series elements in the attenuator are diodes D12 and D13, and the shunt elements D11, D14 and D15. Fig 4.2 below shows the network theoretically, with the diodes represented by resistors. The impedance states refer to a condition of high attenuation.

4.22 Referring to the circuit diagram, Fig. 3, if the a.g.c. voltage drives the anode of D15 positive, then current will flow in R45 and the cathodes of D12 and D13 will be reverse biased, causing a high series impedance. The current in R37 will flow through D11 and that in R48 will flow through D14 causing a low shunt impedance. A low level of a.g.c. voltage will produce the opposite conditions, with variable attenuation over the a.g.c. range.




Theoretical P.I.N. Diode Attenuator Fig. 4·2

Counter Inhibit Circuit ('B' Channel)

4.23 The 'B' channel signal is fed from Q8 via C45 to the $10^0$ counting decade IC25, and also via C46 to a 'level inhibit' stage which automatically inhibits IC25 if the input signal level is too low for reliable counting. The inhibit is produced by IC29a and the threshold is preset by R68. The signal from Q8 is fed via detectors D17/D18 to IC29a/1. The reference voltage at IC29a/2 is preset by R68. If the input signal level is unsatisfactory the output at IC29a/12 will be low which will turn off the inverter Q10. So long as Q10 remains off, IC25 will be inhibited, as described in para. 4.10.

Automatic Gain Control

4.24 At low signal levels the cathodes of D17 and D18 will be approximately 0V. As the signal amplitude increases, the voltage at the cathode of D11 (and also at IC29b/7) will become increasingly negative. When the voltage at IC29b/7 is equal to or more negative than IC29b an output will be applied from IC29b/10 to Q9, which feeds current into the p.i.n. diode attenuator at D15.

$10^0$ DECADE OUTPUTS

4.25 The 'carry' output of IC25 is fed to the input of the next (off-chip) decade in the counting chain (IC6 in Fig.4). The b.c.d. data is fed out on lines A, B, C, D to the data store for the L.S. (least significant) decade which is contained in IC4 (Fig.4).

$10^0$ and $10^1$ Decade Data Transfer

4.26 Referring to the circuit diagram Fig. 4, the 'carry' signal from the least significant decade (Fig. 3 IC25) is fed via shaper IC15d to the input of the high speed decade IC6. The b.c.d. ouput from IC6 is fed to one set of inputs (pins 4, 10, 8 and 6) on IC4.

4.27 IC4 is a CMOS Dual Quad 4-Input Latch with tri-state output. When pin 15 is addressed, the data from the least significant decade (IC25) is transferred to the outputs. When pin 3 is addressed, the data from the next least significant digit ($10^1$) is transferred (IC6). The strobe input pins 2 and 14 receive the unlatch signal (via IC7c) at the same time as the data stores in the CDI Chip (IC5/4). Refer to para. 4.46 for further information.

Data Multiplexing

4.28 The four output lines from IC4 are fed into the 2:1 multiplexer IC11 in which the data from the two off-chip decades is combined in the correct sequence with the $10^2$ -$10^8$ data from the CDI Chip (IC5 pins 15-18). From IC11 the multiplexed data is fed direct to the inputs of the BCD-to-seven-segment decoder IC1 on the Display Assembly.

## SIGNAL INPUT TO CDI CHIP

4.29 After counting in the off-chip decades IC25 and IC6, the input signal is fed to the 'A' channel input at pin 22 of the CDI Chip IC5 (Fig.4).

4.30 IC5/22 is normally low and therefore accepts a 'high' as the carry signal to the internal counting decades. This carry signal is taken from the QD output of the $10^1$ decade IC6.

4.31 The end of the 10th state in IC6 sends the QD output low. This is inverted in IC14f to set the bistable IC3a, sending the 'D' output high and thus providing a 'carry' signal to IC5/22. The 'carry' is terminated by using the QC output from IC6 to reset the bistable via IC19d/12.

## OVERFLOW DETECTOR

4.32 The overflow signal on the 9th state of the data ouput from the CDI Chip is obtainable when IC23 pin 9 goes high. This is clocked through IC7a by the 10kHz (or 5kHz on 'C' channel) multiplexing signal at IC7a/2, which imposes a delay of half a clock period to ensure that the overflow information is not occurring transition.

4.33 The overflow signal is inverted in IC8f and applied to the CLK input of the D-type bistable IC13b, this gives a '1' at IC13b/9 which becomes a '0' at IC24c/6, thus turning on the OVERFLOW/STANDBY indication LP1. The same '0' is fed to pin E of the Remote - BCD option socket SK1 for further processing in PCB Assembly 19-0859. (Option).

4.34 The function of IC8b and D38 is to transfer a brief 'blanking' pulse to IC13b/12 when the collector of transistor (e) in IC26 goes low at the end of each main gate period. This inhibits the overflow indication while the multiplex system is re-synchronising.

## DECIMAL POINT ENCODING

4.35 Decimal point (d.p.) position is determined by combining the time base (x-y-z) logic as given in Table 2 on page Tech. Spec. (7) with the channel selection logic from switch S2A. This data is fed into the 4-Bit Full Adder IC10.

4.36 The outputs EA, EB, and EC from IC10, containing the 'summed' information, are fed to pins 13 to 15 on the 4-to-10 Line Decoder IC2 on the Display Assembly. The 10 line output from (1) IC2 drives the d.p. lines on the display indicators via the limiting resistors on the array IR1. (In circuit diagram Fig.4 components on the Display Assembly are given the prefix '1').

## CHECK, LF and 'C' CHANNEL SIGNAL GATING

4.37 Referring to Fig. 4, these signals are gated via the network formed by IC9 and IC15c, controlled by logic applied either by the local front panel switches S2, S50 and S51 (option), or by remote control.

4.38 The selected signal is fed from IC9/8, via the TTL-to-ECL converter Q37, to the base of Q6 (Fig.3) in the 'A' channel output path.

4.39 When LF mode is selected, the switch S51 applies to '0' to IC19b/5. This, via IC19c and IC24b applies a '1' to IC15c/8. The resulting '0' at IC24a/2 is converted to a '0' at +5V ECL level by the potential divider R88, R89 and R90, and applied via the line 'A Inhibit' to IC21c/11 (Fig.3) to inhibit the 'A' channel output during LF measurement. The 'A' input is used for LF but the signal is extracted at Q4 and fed to the LF Multiplier p.c.b.)

## TIME BASE (GATE TIME) SELECTION

4.40 The time base decade divider chain is contained within the CDI Chip and is programmed via the x-y-z lines on pins 8, 9 and 10 of IC5. The logic program for application to these lines is given in Table 2 on page Tech Spec (7).

4.41 The x-y-z program is supplied from the local GATE TIME switch S1 via the open-collector gates IC16a, b and c, or, when on remote control via pins 11, 7 and 10 of the Remote/BCD Option socket SK1.

4.42 When remote control is in use, the Remote Command line (pin 2 of SK1) is held at logic '0', thus disabling IC15a, b and c and isolating the local GATE TIME switch.

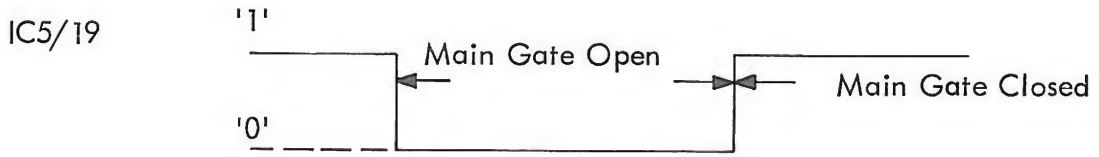
## CONTROL AND UPDATE

### Main Gate Output

Fig.4

4.43 The main gate waveform, generated within the CDI Chip, is fed out on IC5/19 to synchronise the off-chip decades and initiate the start of the display time. The relevant circuitry is centred on IC12a, IC12b, IC17b and IC17a.

4.44 When the main gate opens to start a measurement, pin 19 of IC5 goes 'low':-




This is inverted in IC14b and fed via D20 (Fig.3) as a '1' to the 'D' input of IC20, thus removing the inhibit from the $10^{o}$ decade IC25 and allowing measurement to commence.

4.45 At the end of the main gate period IC5/19 goes high. The inhibit is re-imposed on IC25, thus stopping the count. The stored data is now released, as follows:

Data Transfer and Off-Chip Reset

4.46 When the main gate closes, the 'high'at IC5/19 clocks IC12a/3, causing the $\overline{Q}$ to go to a '0'. This, via IC7c, transfers the off-chip decade information to the latches within IC4.

4.47 The 10kHz (5kHz in 'C' channel) multiplex reference signal via IC18d then clears IC12a $\overline{Q}$ to a '1'. This clocks IC12b $\overline{Q}$ to a '1' which via IC19a clears the two off-chip decades.

4.48 The '1' at IC12b $\overline{Q}$ is fed via IC19a, IC14e and IC19d to IC13a, which clears the carry circuit for the CDI Chip.

Display Time Generator

4.49 The display time generator is formed around transistors Q11, Q12 and Q13, the display time period being determined by the time constant of the charging path Q13, R107, R106 into C63. During the measurement period (main gate open) IC18a/2 is a '0' and this shunts C63, thus inhibiting the display time generator.

4.50 When the main gate closes, the positive going edge on IC17b/3 forces the $\overline{Q}$ to a '0' which places a hold signal on IC5/13 and produces a '1' at IC18a/2, removing the shunt from C63. The capacitor then charges up towards +5V.

4.51 C63 charges until the voltage on Q12 emitter is more positive than the base, at which point Q12 starts to conduct, feeding current into Q11 base. Q11 now turns on, which causes Q12 to conduct more heavily and this very rapid regenerative action turns both transistors hard on, allowing C63 to discharge via R105.

4.52 The very rapid turn on of Q11 produces a narrow-going pulse at the collector which is applied to IC17b/1 and forces the $\overline{Q}$ of IC17b to '1'. This produces a '0' at IC18a/2 which restores the clamp on C63, and releases the hold via IC7d on IC5 pin 13, resetting the counters in the CDI Chip, as described in para. 4.54.

4.53 A remote 'counter hold' can be obtained by a '0' on pin F of socket SK1. This is inverted in IC18b and reverse biases Q13, thus preventing any charging of C63.

Automatic Reset

4.54 The counting decades within the CDI Chip can be controlled by logic levels applied to pin 13 of IC5 as follows:-

IC5/13 ( Hold ..... '1'
( Free run ..... '0'
( Reset ..... Transition '1' to '0'

4.55 The Hold condition ('1') is applied while the display time generator is charging C63, and an automatic reset transition is obtained when Q11 and Q12 turn on, as described in para .4.51. While the display time generator is quiescent the $\overline{Q}$ output of IC17b applies a '0' to IC5/13, thus allowing the counters to run free during the main gate open period.

4.56 The reset pulse at IC7d/11 is also fed via C70 to the base of transistor (e) in IC26, to clear the overflow system and briefly blank the display during the reset pulse.

Manual Reset

4.57 The RESET Position of the CHECK/OPERATE/RESET switch S50 allows the user to interrupt a gate time at any instant and initiate a new measurement. The RESET position of the switch is spring-biased, and the reset action occurs at the moment of release.

4.58 When the CHECK/OPERATE/RESET siwtch S50 is put to the RESET position, and then immediately released, the following reset actions occur:-

(1) IC17a is cleared and the 10kHz reference (5kHz in 9921 channel 'C') at IC17a/11 clocks the bistable.

(2) The resulting negative edge at IC17a/18 is differentiated to give a narrow pulse which is fed via IC18f to:-

(a) Via IC18c to clear IC17b which produces a reset pulse for the CDI Chip similar to that described for Q11 collector (para.4.52)

(b) Via IC18e and IC7c to reset the strobe inputs at IC4 pins 2 and 14.

(c) Via IC19a to clear the off-chip counter circuitry IC6, IC13a and IC25 (Fig.3)

(d) Applies a '0' to pin 4 of the CDI Chip to unlatch the data stores.

(e) Via IC7d/11, C70 and IC26(e) to reset the overflow system and briefly blank the display.

DATA OUTPUT AND DISPLAY SYSTEM Fig. 4

Display

4.59 The Display Assembly contains a 9-digit numerical display using l.e.d. indicators D11-D19. The b.c.d. data is converted by a 7-segment decoder IC1 and the required l.e.d. indicator is turned on by the associated driver transistor Q21 to Q29. In the circuit diagram (Fig.4) components on the Display Assembly one given the prefix '1' for identification.

## Multiplex System

4.60 The complete readout cycle consists of 10 states, each of 100μs*, timed by a 10kHz reference frequency. The 10kHz* reference interrogates each decade store for 100μs* and releases the data in the correct sequence to the 7-segment decoder. At the same time the corresponding l.e.d. driver transistor in the display is turned on for 100μs* to illuminate the correct numerical l.e.d. for that state. The system is synchronised by a pulse Ro generated in the CDI Chip, and fed out on pin 14 of IC5.

4.61 The display data from the two off-chip decades is combined, with the data from the CDI Chip, in the 2-to-1 multiplexer IC11. This data is then fed to the BCD-to-7 segment decoder (1) IC1 in the Display Assembly.

4.62 Correct sequencing of the data in the multiplexer IC11 is achieved by feeding selection signals into IC11 pin 1 from pins 6 and 9 of IC23. These two lines enable the $10^0$ and $10^1$ data transfer. The $10^2$ - $10^8$ data from pins 15 to 18 of the CDI Chip is already correctly sequenced by the 10kHz multiplex reference signal within the Chip.

## Display Drivers

4.63 The multiplex reference frequency from IC5/14 provides the clock input at pin 13 of the ripple counter IC23. The 100μs pulses [illegible] in turn the transistors in IC27 and IC26 in sequence, and thereby enable each driven transistor, Q21 - Q29 in turn.

## LED INDICATORS

### Overflow/Standby Indicator LP1

4.64 During normal operation this l.e.d. illuminates when the overflow detector puts a '0' on IC24c/6. When the instrument is put into the 'standby' condition, however, the l.e.d. is illuminated continuously because, with the +5V output from IC51 switched off, the other indicators (LP2 to LP5) are without power and current in LP1 can thus find an earth via D1 and R3.

### MHz and Hz Indicators:- LP2 and LP3

4.65 The path through R137 will be a '0' for all measurement modes except 'LF', thus illuminating LP2. When LF Option mode is selected the logic from the switches S2b, S50 and S51, via IC28b and IC24b, will turn on LP3.

* The multiplex reference is 5kHz and interrogation time 200us in 9921 when using 'C' channel.

Gate Indicator LP4

4.66 The negative going main gate open signal at pin 19 of the CDI Chip is inverted in IC14a and IC24e to turn on LP4 during measurement periods.

External Standard Indicator LP5

4.67 This is turned on by a '0' at IC3c/6 when Q31 is turned on by the detected external standard signal.

Overload Indicator LP50

4.68 This indicator is described in para. 4.20

FREQUENCY STANDARD INPUTS

Frequencies

4.69 The internal frequency standard is 5MHz but this is divided down to 1MHz in the 9918 and on channels A and B of the 9921. On channel 'C' of the 9921 the frequency standard is further divided down to 500kHz. These frequencies are fed into the CDI Chip at IC5/20.

Internal Frequency Standard

4.70 The alternative 5MHz standards are listed under Options 04A, 04B and 04B and 04C on pages Tech. Spec. (3) and (4). The output of the 5MHz oscillator is fed via shaper Q30, the $\div 5$ counter IC2a and the Internal/External selection gates IC1b/5 and 1C1a/8, to the CDI Chip at IC5/20.

Automatic Changeover

4.71 When the 1MHz external frequency standard is applied to the rear panel EXT STD I/P socket, the instrument automatically changes to external standard operation and the indicator LP5 illuminates, as described below.

External Standard Input

4.72 The 1MHz applied to the EXT STD I/P socket SK52 is fed via Q32 to the Schmitt trigger IC3a. The output at IC3a/2 is fed to the gate IC1b/2 and also to the detector D23/C74. The detected signal turns on Q31, thus causing a low at the collector and a '1' at IC1b/3. This allows the external standards to pass through the selection gates to the CDI Chip. At the same time gate IC1b/4 is disabled by a '0' from inverter IC3c/6, thus inhibiting the external standard and turning on the indicator LP5.

Internal Standard Output

4.73 Whichever frequency standard is in use, the 1MHz at IC1b/6 is fed via inverter IC3e and R146 to the rear panel socket SK53.

500kHz Frequency Standard (9921)

4.74 The 1MHz at IC1b/6 is fed to the ÷ 2 counter IC2b but the 500kHz output is held at IC1a/10 unless 'C' channel is selected, in which case switch S2a puts a '0' on IC1a/2 which inhibits the 1MHz signal. The same logic puts a '1', via IC3d, on to IC1a/11, which enables the 500kHz path to the CDI Chip. The reason for using the 500kHz frequency standard is that it effectively converts the division by 200 in the 3GHz section into the required division by 100.

FREQUENCY STANDARD OPTIONS

4.75 These are listed in the Technical Specification as 04A, 04B and 04C. The instrument is normally supplied with 04B. The circuit and component layout diagram for Option 04C is Fig. 12. No technical information is provided for the ovened as these should be serviced only by Racal Instruments Ltd, or authorised agents. A frequency calibration procedure is given in Chapter 5.

POWER SUPPLY

AC Supply

4.76 The a.c. supply is connected via a mains lead (power cord) supplied with the instrument, which plugs into the combined filter-connector mounted on the rear panel. The supply is then fed via the rear panel anti-surge fuse FS350 to the front panel POWER ON/OFF switch.

4.77 With the POWER switch at ON, the a.c. supply is fed via the voltage selector switches S52 and S53 (Chapter 5 Para. 5.5 ) to the primary of mains transformer T1, which has three secondary windings providing nominal regulated outputs of +5V, -10V and +24V respectively.

+5V Supplies

4.78 The nominal +5V supply is rectified by the encapsulated bridge D50m which is mounted on the rear panel for adequate heat dissipation. Regulation is by two integrated circuit voltage regulators IC50 and IC51, which are mounted on the side panel. These packages contain all the required voltage regulating and current limiting functions.

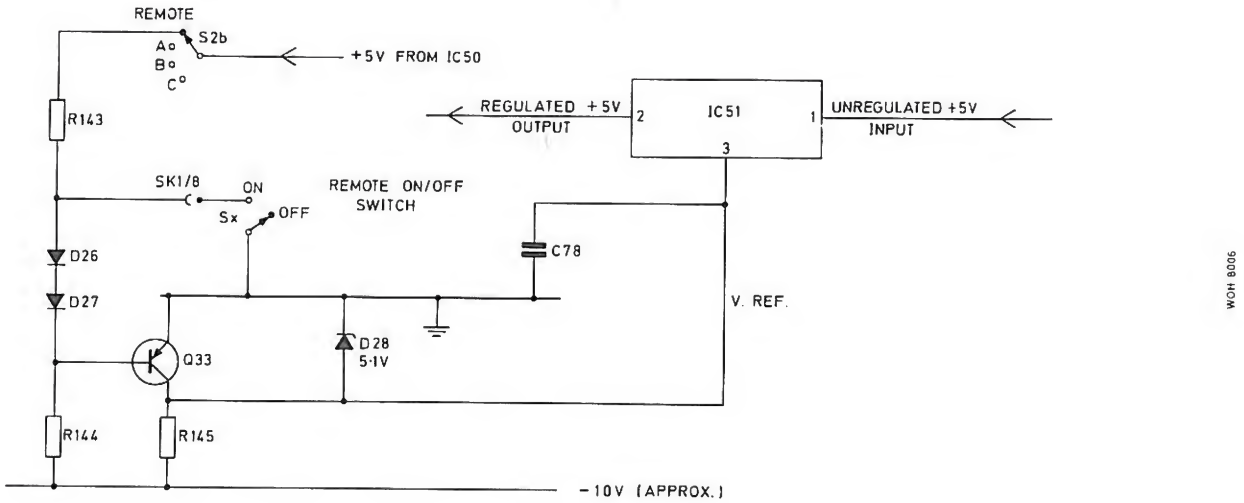
4.79 IC50 regulates the +5V supply for the 'A' and 'B' channel amplifiers and the internal frequency standard; also for the 3GHz section (9921). The amplifier and 3GHz +5V supplies are switched via Q17, Q18 and Q20, according the setting of INPUT switch S2a.

Standby

4.80 IC51 regulates the +5V logic supply. The output of this regulator is switched off whenever the unit is in the standby condition, as follows.

4.81 When operating locally (remote control system not connected or not programmed). Standby is obtained by setting the INPUT switch to the REMOTE position. This inhibits the regulator IC51 in the following manner.

4.82 Fig.4.3 below, shows part of the power supply circuit in Fig.4. The switch contact Sx represents the power 'on' switch in an external remote control system. When remote control is not fitted, Sx is effectively an open circuit.




+5V Switching in Standby Mode Fig. 4.3

4.83 Assuming that Sx is an open circuit, and that the local INPUT switch S2b is set to REMOTE, current will flow from the +5V output of IC50 through D26/D27 and reverse bias the base-emitter junction of Q33. With Q33 turned off, the zener diode D28 conducts and applies -5.1V to the V ref. line at IC51/3. This negative reference inhibits IC51 and reduces the output at IC51/2 to 0V, thus cutting off the voltage to the instrument's logic system.

4.84 When the local INPUT switch S2b is not on REMOTE, there is no current flow in D26/D27 and Q33 conducts, thus connecting the V ref line to 0V, which removes the negative inhibit from IC51. The same effect is obtained in REMOTE control by closing switch Sx which bypasses D26/D27.

### -5.2V and -10V supplies

4.85 Rectification is by the discrete diode bridge D29-D32 and regulation of -5.2V is carried out by IC52. The -5.2V supply is fed to the 'A' channel amplifier via Q16. Approximately -10V is obtained from the rectifier and this is used in the 3GHz Section (9921) and switched via Q19.

### +24V Supply

4.86 Rectification is by the discrete diode bridge D33-D6 and regulation is carried out by IC34. This supply is used in the 3GHz section of the 9921.

### CDI Chip 2V Supply

4.87 A stabilized +2V supply is derived from the unswitched +5V rail via the regulator Q14, which is controlled by Q15 from a reference voltage supplied from the CDI Chip at IC5/11.

## LF MULTIPLIER OPERATION (OPTION)

### Signal Path

4.88 The signal for the LF Multiplier is taken from the collector of Q4 in the 'A' amplifier (Fig.3) and processed in the LF Multiplier p.c.b., after which it is fed back to the main p.c.b. at pin 34 and directed through the selection gates in IC9 (Fig.4) whence it is fed via Q37 to the input of the $10^{\circ}$ decade IC25.

## LF MULTIPLIER ASSEMBLY 19-0797 (Fig.6)

### Principle

4.89 Frequency multiplication is achieved by a voltage controlled oscillator which by means of a link can be set to run at either 50 times or 100 times the input frequency. The divided oscillator frequency is phase-compared with the input frequency to provide fine control of the oscillator frequency.

Circuit Description

4.90 The LF signal is fed from Q4 in the 'A' amplifier (Fig.3)into the LF Multiplier p.c.b. Referring to the LF Multiplier circuit (Fig. 13) the signal is fed via C1 into the Operational Amplifier IC1, which functions as a Schmitt Trigger. With an input of approximately 400mV peak-to-peak applied to IC1, an output of approximately 6V peak-to-peak will be fed into IC2/14.

4.91 IC2 contains a voltage-controlled oscillator (VCO) in a phase-locked loop (PLL). The factors controlling the oscillator frequency are:-

(1) The voltage on pin 9 of IC2.

(2) The resistance between pin 11 and the negative rail.

(3) The capacitance between pins 6 and 7.

(4) The output of the phase comparator at pin 13.

4.92 The oscillator output at IC2/4 is fed via Q3 to a divider chain (IC3 and IC4). The divider signal is fed back via Q2 to pin 3 of IC2, where it is compared in phase with the original signal in pin 14. This phase comparison voltage is fed out via pin 13 and R4 to pin 9, to pull the oscillator to a frequency which is a precise multiple of the input frequency.

4.93 The link on the divider IC3 can be set for division either by 5 or by 10. In the 9918 and 9921 it should be set in the LK2 position, for division by 10 thus giving a multiplication factor of 100 to the input signal.

# CIRCUIT DESCRIPTIONS 3GHz SECTION (9921)

## TOP LOOP AND SAMPLER ASSEMBLY 19-0856

### Introduction

4.94 The circuit diagram for this Assembly is on two sheets. Figure 6 contains the Dual Sampler Sub-Assembly 19-0752 together with the pulse generators and output buffers. The remainder of the 3GHz section is shown in Figure 7, which contains the oscillator for the top loop (VCO 1) together with the loop filter and sweep speed-up circuit. A simplified block diagram of the 3GHz section is shown on page 3-7.

### Pulse Generator and Sampling Mixer SM1

4.95 The sampling mixers on sub-assembly 19-0752 are identical, therefore only Sampling Mixer No. 1 (SM1) will be described. Refer to Fig. 6 at the back of the book.

4.96 Consider first the input from VCO 1 to SM1. This oscillator signal is applied via R75 (Fig.7) and C1 (Fig.6) to the limiting amplifier Q1 which feeds the long-tailed pair Q3/Q2. Transistor Q2 drives the transformer T1 which has a centre-tapped secondary driving the pulse generator D1, which is mounted on the sampler sub-assembly 19-0752.

4.97 The step recovery diode D1 produces very narrow pulses which are applied in anti-phase via C4 and C5 to turn on the sampling diodes D2 and D3, which are part of a matched quad with D5 and D4.

4.98 The 'C' channel input signal is applied via C6 and attenuator R9/R6 to the sampling diodes. If the pulse generator p.r.f. and the input frequency are harmonically related the mean charge on C4 and C5 will be constant, thus feeding a steady d.c. voltage to the output buffer Q7a/Q8.

### Output Buffer Amplifier for SM1

4.99 Transistor Q7a/Q7b is a dual FET in one envelope. The +11V supply is obtained from the +24V supply, which is reduced to +11V and regulated by Q33 and associated circuit (see Fig.7).

4.100 Q7a operates as a source-follower feeding the sampler output via R27 to pins 7 and 8 of the p.c.b. Q8 is an emitter follower which improves the frequency response of the buffer by bootstrapping the feedback capacitance of the FET.

4.101 Since Q7a does not operate at zero Vgs, the circuit of Q7b is provided to give the required volt drop for correct biasing of the loop filter. The bias level is adjustable by R8, which has the effect of determining the sweep speed of integrator IC1 (Fig.7). To ensure correct biasing over a wide temperature range Q7b is controlled by a voltage produced in the Digital Offset Compensator Assembly 19-0871 (generally referred to as the Compensator board). The functions of Q7a, Q7b and R8 are referred to again when explaining the action of Compensator Board 19-0871.

4.102 The buffer output from pin 7 of the p.c.b. is fed via link LK2 to the integrator input of the top loop filter (via R42 in Fig. 7).
From pin 8 the output is taken to the sweep speed-up circuit (via C51 in Fig.7).

Sampling Mixer No. 2 (SM2)

4.103 Sampling Mixer SM2 functions in the same manner as SM1.
The external signal enters via C7 and the oscillator signal from VCO 2 (see Fig.7) is applied via R21/C14.

Output Buffer Amplifier for SM2

4.104 The output buffer Q9/Q10A functions in a similar manner to Q7A/Q8, except that it is supplied from the +5V line and Q10A operates with zero Vgs.

4.105 The source-follower output from Q10A is fed via R32 and pin 17 to the processor circuit in 19-0857 (see Fig.8).

Top Loop Oscillator, Loop Filter and Sweep

4.106 The circuit diagram is Fig.7.

4.107 Summary The Loop Filter is formed, basically, by integrator IC1, emitter follower Q13 and associated components. Sweep reset action is provided by IC2, Q14 and Q12. Transistors Q31 and Q32 provide TTL compatible signals to the Compensator board. The circuit around Q33 forms the +11V regulator.

4.108 The oscillator (VCO 1) is Q17 with separate outputs via Q19 and Q30.
The remainder of the circuit across the bottom of the diagram, is concerned with the sweep speed-up process.

Loop Filter and Sweep Circuit

4.109 The 'difference' signal produced in Sampling Mixer SM1 (Fig.6) is fed via R42 to the summing junction at IC1 pin 2. The integrator IC1 provides a sweep action; the sweep rate being controlled by the Compensator board, with adjustment by means of R8 (Fig.6) which determines the bias (Integrator offset) applied to pin 3 of IC1. To ensure an adequate input dynamic range, IC1 is operated from an 11V supply via regulator Q33 and associated components.

4.110 The function of IC2, Q14 and Q12 is to provide a rapid reset at the end of each tuning sweep, the circuit action being comparable to that of a Schmitt trigger, as follows:

4.111 The basic sweep action is a slow sweep down followed by a rapid reset, this cycle being repeated continuously during the search period. When the downward sweep at Q13 emitter reaches the lower limit it causes the output of IC2 to change state, which turns on Q14 and Q12. The resulting current in Q12 is drawn from the summing junction at IC1/2. This causes a rapid rise (reset) in the level at Q13 emitter. When the upper threshold is reached, the output of IC2 falls, turning off Q14 and Q12. The slow downward sweep is then repeated.

Function of Q13

4.112 If the sweep signal at IC1 pin 6 should rise above +3.4V (approximately) it turns on Q31. This sends Q31 collector high and provides the 'Ramp Up'signal for use in the Compensator board (para.4.127). Zener diode D11 fixes the operating point for Q31.

Function of Q32

4.113 As described in para.4.111, IC2 provides an output which resets the integrator at the end of each sweep. This signal is converted to a TTL compatible level by Q32, for use in the Compensator board.

Function of Q11

4.114 Q11 is an a.c. coupled amplifier which accepts the sampling mixer signal and provides an r.f. bypass to ensure good h.f. response in the oscillator control path.

Voltage Controlled Oscillator (VCO 1)

4.115 The oscillator is Q17 operating in a Colpitts-type circuit, tuned by L12 and the voltage variable capacitance (varactor) diode D5.
A sweep tuning control is applied from the integrator output IC1/6 via emitter follower Q13 and link LK3.

4.116 Two oscillator outputs are provided. The output via Q18 collector feeds the limiting amplifier Q19 which supplies a shaped waveform to the ÷ 400 digital divider on p.c.b. 19-0857 (Fig.10). The output from Q18 emitter is fed via Q30 to the pulse generator of the Sampling Mixer SM1 (via C1, Fig.6).

4.117 A regulated supply rail for the oscillator, derived from the -7.5V d.c. line, is provided by Q15, Q16 and associated components.

## Sweep Speed-Up Circuit

4.118 Summary The sweep speed-up circuit receives an output from sampling mixer SM1 via C51. If this mixer output contains a beat frequency higher than about 1MHz this is detected by a frequency discriminator which activates a Schmitt Trigger circuit. This triggering of the Schmitt allows current to flow into the summing junction of the integrator at IC1/2, thus greatly increasing the sweep speed.

4.119 The increased sweep speed is maintained until the beat frequency output from the sampling mixer falls below 1MHz, at which point the output of the frequency discriminator falls to a level which allows the Schmitt to return to its original state. This cuts off the flow of current into IC1/2, causing the sweep speed to revert to the normal rate.

4.120 Circuit Details The relevant parts of the speed-up circuit are the low-pass filter between buffer transistors Q20/Q21, and the compensating amplifier Q22. Transistors Q23, Q24 and Q25 form a limiting amplifier which provides signal drive to the frequency discriminator.

4.121 The frequency discriminator D9/Q26/C70 is of the diode/transistor pump type which controls the action of Schmitt Trigger Q27/Q29 and Q28. The collector of Q27 is fed from +11V to supply adequate current to IC1/2.

4.122 In the 'slow sweep' condition the Schmitt condition is such that Q28 will be conducting heavily. If, however, the frequency discriminator input rises above 1MHz (approximately) the Schmitt will turn off Q27 and Q28, thus feeding current via D14 and R16 into the summing junction at IC1/2, which increases the sweep speed.

4.123 A TTL compatible sweep speed-up output for the Compensator board 19-0871 is taken from the collector of Q28, this turns on the oscillator and counter in 19-0871.

## DIGITAL OFFSET COMPENSATOR ASSEMBLY 19-0871

### Introduction

4.124 The circuit diagram is Fig. 8, and the assembly will be referred to as the Compensator board. The purpose of the Compensator circuit is to maintain the correct offset bias at the input to the top loop integrator IC1 in 19-0856 (Fig.7) thus ensuring a constant ramp rate under varying temperature conditions.

4.125 The Compensator circuit consists essentially, of an 8-bit counter and a digital-to-analogue (D/A) converter in a single CDI Chip IC5, together with an oscillator and control circuitry. A compensation cycle is triggered by certain conditions in 19-0856, and ends when the two inputs to integrator IC1 (Fig. 7) are equal. This compensation cycle can only occur when the top loop is not in lock.

Circuit Description

4.126 The circuit diagram of the Compensator board is Fig.8, but the description also refers to Fig.6 and Fig.7.

Referring to Fig.8, a compensation cycle commences if a triggering signal is received on any of the control inputs 'Sweep Reset','Sweep Speed-Up' or 'Ramp Up'. This signal applies a reset signal to the counter in IC5 and also to the bistable IC3c/IC3d. The inputs via pins 4 and 5 are differentiated by R1/C5.

4.127 When the counter is reset it causes the output (IC5/14) from the D/A section to fall to approximately 0V. At the same time the oscillator IC4a/IC4b is enabled by the bistable and starts to clock the counter. This produces a staircase waveform output rising towards approximately +2.5V.

4.128 The D/A output is fed to IC2, which with the resistor network R3, R4 and R5 shifts the minimum bias level down to -0.25V and divides the step size by a factor of five; thus the bias which is fed to the gate of Q7b (19-0856 Fig.6) has a range of -0.25V to +25V.

4-129 If there were no input to IC1, the Compensator board count in IC5 would reach 255, then reset and repeat the cycle.

However, referring now to Fig.6, if the bias input to the gate of Q7b brings the sources of Q7a and Q7b to virtually identical levels, it will cause the reference voltage which is applied to IC1/3 in the Compensator board to be equal to that on IC1/2. This will send the output at IC1/6 low, which changes the state of bistable IC3c/IC3d, thus stopping the oscillator IC4a/IC4b. This halts the change of d.c. voltage from the D/A converter and holds the bias output from IC2/6 at the required level.

4-130 The bias level from IC2/6 is fed to the gate of Q7b (Fig.6) and thus (with Q7a) causes a fixed voltage difference to appear at the integrator inputs (IC1 in Fig.7) thereby determining the correct ramp rate and sensitivity. The required bias level, and hence the ramp rate, is set by R8 (Fig.6).

2nd LOOP AND OUTPUT PROCESSOR ASSEMBLY 19-0857 (Figs.10 and 11)

Introduction

4.131 The circuits for the 2nd Loop are shown in Fig.10 and those for the Output Processor in Fig.11. The 2nd Loop will be described first. The frequency symbols $F_1$ and $F_2$ refer to the description in Chapter 3. To gain access to the component side of the p.c.b's in the 3GHz section, this p.c.b. must be partly detached, as described in Chapter 6.

2nd Loop Oscillator and Division System (Fig.10)

4.132 Referring to Fig.10 the circuit comprises the ÷ 400 circuit on the left, the ÷ 399 circuit on the right and the frequency and phase comparator in the centre. Below is the oscillator VCO 2 which is identical to VCO 1 in Fig. 7.

4.133 The output from the Top Loop oscillator VCO 1 is fed into the p.c.b. at pin 8 and is applied to the limiting amplifier Q5 which gives a TTL output for driving the divide-by-400 chain IC6, IC7 and IC8.

4.134 The frequency and phase comparator is IC4, the signals $F_1/400$ being fed into IC4/1 and $F_2/399$ to IC4/3. These two signals are compared and any 'error' signal is fed via the loop filter IC5 and link LK1 to the oscillator tuning vacactor D5. This error signal will automatically tune the oscillator Q3 to eliminate the frequency 'error'. No sweep system is required.

4.135 One of the oscillator outputs is fed via the collector of Q4 to the limiting amplifier Q7 which applies a squarewave drive at TTL level to the ÷ 399 chain IC1, IC2 and IC3.

4.136 The ÷ 399 chain is arranged as a 'swallow' counter. The feedback via AND gates IC9a and IC9b arranges that the count is terminated one count short of the full 400.

4.137 From IC3/11 the ÷ 399 output is fed to the comparator at IC4/3 as previously described.

4.138 A second output from the oscillator is fed via Q6 emitter and pin 1 of the p.c.b. to the pulse generator of Sampling Mixer SM2 (Fig.6).

Output Processor Circuits

4.139 The Output Processor receives the output from Sampling Mixer SM2 ($f_x/400$) and applies the following processes:-

(a) Signal filtering.

(b) AGC.

(c) Frequency doubling.

(d) Low input detection and inhibit.

4.140 Filtering. Referring to Fig. 11 the processor input signal ($F_x/400$) which can range in frequency from 0.75MHz to 7.5MHz, enters the p.c.b. at pin 12, is buffered by Q12 and then filtered by the 7.5MHz low-pass filter (L10,L11 and associated components) to remove unwanted signals.
The filtered signal is then supplied to the a.g.c. circuits via the compensating amplifiers Q14 and Q15.

AGC

4.141 The a.g.c. loop is formed by transistors Q16 to Q21, peak detector D10 and d.c. amplifier IC10.

4.142 Transistors Q17 and Q18 form a long-tailed pair with a fixed bias on Q18 and variable a.g.c. bias (via IC10) on Q17. The magnitude of signal which can pass from Q16 to Q18 is determined by the bias on Q17.

4.143 Transistors Q19, Q20 and Q21 provide buffering and amplification. The signal from Q21 emitter is fed via C55 to the peak detector D10/C54. The detected signal is applied via D9 to the d.c. amplifier IC10 which has a nominal gain of 100.

4.144 The d.c. output level at IC10/6 determines the conductivity of Q17. Potentiomater R59 controls the flow of current into the summing junction at IC10/2 and can thus preset the signal level at the emitter of Q21.

4.145 Frequency Doubler. From Q21 emitter the level-controlled signal is fed to amplifier Q24 which has a gain of x 10. From Q24 collector the signal is fed to the Schmitt shaper IC11a which supplies a square-wave signal to the frequency doubler chain IC12d to IC13d.

4.146 The frequency doubler functions by producing a pulse from each edge of the square-wave input, thus doubling the p.r.f.
The doubler output is fed via inverter IC13b and R78 to the 'C' channel path on the Main p.c.b. (Fig.4).

4.147 Low-Level Detection and Inhibit. An output from the a.g.c. amplifier at IC10/6 is fed via R65 to a Schmitt Trigger Q22/Q23.
With a very low signal at the 'C' channel input the d.c. level at IC10/6 will drop to approximately -4V or lower. This increasingly negative level will be detected by Q22/Q23 which will apply a logic '0' to the input of the frequency doubler at IC12d pin 12, thus cutting off the doubler drive and inhibiting the 'C' channel measurement process.

# CHAPTER 5

# MAINTENANCE

## INTRODUCTION

5.1 This chapter describes test procedures for both the 9918 and 9921. The information up to and including paragraph 5.21 refers to both models. The remainder of the chapter applies only to the 9921.

TABLE 6

LIST OF TEST EQUIPMENT REQUIRED

| Item | | Description and Examples |
|---|---|---|
| 1 | Digital Multimeter | Range 0-20V: resolution 10mV<br>Accuracy 0.5% (Racal 9079) |
| 2 | Oscilloscope with<br>x 10 probe<br>x 1 probe with HF tip: | D.C. to 50MHz bandwidth 5mV/cm sensitivity. Sweep rate down to 1 sec/cm |
| 3 | 1MHz Frequency Standard: | Accurate to ± 1 part in $10^9$, nominally 1V r.m.s. (Racal 9475). |
| 4 | Signal Generators: | Frequency range 10Hz to 3GHz.<br>Output level 1mV - 1V r.m.s. into 50Ω<br>Signal/Noise ratio must be better than 40dB.<br><br>Examples<br><br>10Hz - 100kHz Racal 9061/9062/9063/9064<br>100kHz - 550MHz combination.<br><br>450MHz - 1GHz HP.612A<br>800MHz - 2.4GHz HP,8614A<br>1.8GHz - 4.5GHz HP,8616A |
| 5 | Millivoltmeters | Frequency 10kHz to 1GHz<br>Range 1mV to 3V r.m.s. (Racal 9301A) |
| 6 | Universal Counter Timer: | Frequency measurements up to 50MHz.<br>Ratio measurements up to 20MHz on HF channel, 50kHz on LF channel. 1V sensitivity (Racal 9901,9903 or 9905) |

TABLE 6 (Continued)

| | | |
|---|---|---|
| 7 | Ancillary Items | |
| | Terminating Pad | BNC 50Ω |
| | 9921 only | |
| | Coaxial Lead (50Ω) | BNC to 'open end', 1 metre approx. |
| | Coaxial Lead (50Ω) | BNC to 'open end', with terminating network as shown in paragraph 5.37 1 metre approx. |
| | Coaxial Lead (50Ω) | Type N to Type N. 1 metre approx. Type N plugs at both ends of RG 213U cable. |
| | Coaxial Lead (50Ω) | BNC to 'open end' with 56Ω resistor connected across open end. |
| | Resistors: | 100Ω ± 10%<br>680Ω ± 2%<br>56Ω ± 5% |
| | Capacitors: | 0.1μ + 20%<br>680p ± 2% |
| | Resistors and Switch | See para. 5.32 test circuit. |

## REMOVAL OF COVERS

WARNING: DANGEROUS AC VOLTAGES ARE EXPOSED WHEN COVERS ARE REMOVED WITH AC SUPPLY CONNECTED. COVERS SHOULD BE REMOVED BY AUTHORIZED PERSONS ONLY.

5.2 (1) Set the power switch to OFF, switch off the a.c. supply at the supply point and unplug the power lead.

(2) Remove 4 screws from the top and bottom covers. Remove the rubber plugs (located near to the rear end) from both side panels of the instrument and slacken, by about two turns, the screws revealed.

(3) Grip the rear panel assembly and ease it back from the main case to the maximum extent possible (about 5mm).

(4) The rear edge of either cover can now be lifted and the cover withdrawn outwards and rearwards. To replace the covers reverse the above procedure.

## POWER SUPPLY PREPARATION

### Power Lead

5.3 Fit a suitable plug to the power lead supplied in accorance with the standard colour code:

| | |
|---|---|
| Brown | Line |
| Blue | Neutral |
| Green/Yellow | Earth (ground) |

### Supply Fuse

5.4 Check that the rear panel fuse is correctly rated for the a.c. (mains) supply voltage, as follows. The fuse is a glass cartidge, 5 x 20mm, surge resisting type.

| Supply Range | Fuse Rating | Racal Part No. |
|---|---|---|
| 188V - 265V | 160mA anti-surge | 23-0019 |
| 94V - 127V | 315mA anti-surge | 23-0032 |

### AC (Mains) Voltage Selection: General

5.5 The primary of the internal mains transformer is arranged to suit the local a.c. supply by means of two rear-panel slide switches S52 and S53. On earlier models these switches operate in the vertical plane and are secured by a locking plate with a cutaway portion showing the voltage range selected. Instructions for setting this type of selector is given in para. 5.6. In later models the switches will operate horizontally, and be protected by a transparent plastic cover. This type of switch can be recognised by the four positions W-X Y-Z, as illustrated in para. 5.7.

### AC (Mains) Voltage Selection (Earlier models)

5.6 AC supply voltage selection is by means of two vertical slide switches with locking plate on rear panel.

(1) Observe the voltage range marking shown in the cutaway portion of the locking plate. If this is not correct for the local supply, proceed as follows:-

(2) Unplug the power cable from the supply and extract the two screws securing the locking plate and remove the plate.

(3) Refer to Table 7 below and set the slide switches to the positions for the required voltage range. The switches are referred to as left hand and right hand as seen when viewing the rear of the instrument. The references S52 and S53 are visible when the plate is removed.

(4) Ease the plate over the slide switches such as to align the screw holes. Secure the plate with two screws previously removed.

(5) Verify that the cut-away in the plate allows the required voltage range marking to be seen.

TABLE 7

Mains Voltage Selection Switches (Early Models)

| Switch Settings* | | Instrument Voltage Range For Local AC Supply |
|---|---|---|
| Left Hand Switch (S53) | Right Hand Switch (S52) | |
| Up | Up | 94V to 115V |
| Up | Down | 112V to 127V |
| Down | Up | 188V to 230V |
| Down | Down | 225V to 265V |

*Left hand and right hand are seen when looking at the rear of the instrument.

AC (Mains) Voltage Selection (Later Models)

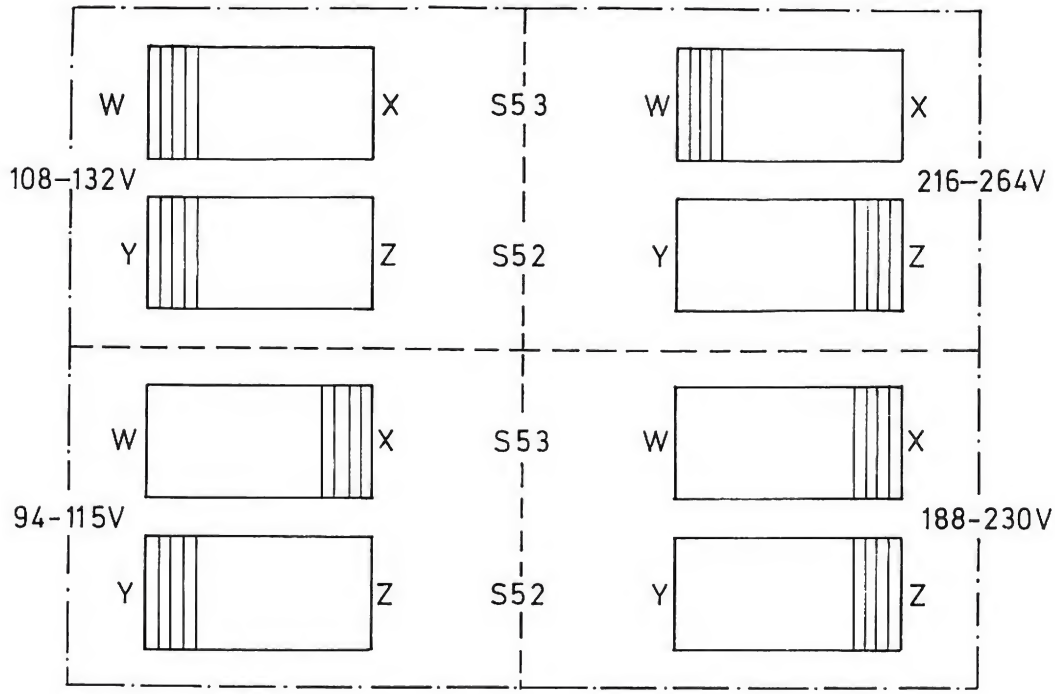
5.7 (1) Remove the transparent cover (two screws) from the switches and set them to the appropriate positions W or X, Y or Z, for the required voltage range, as shown in Fig. 5.1.

POWER CIRCUIT RESISTANCE TESTS

5.8 (1) Do not connect the a.c. mains supply.
Check that the mains fuse is correctly rated for the supply voltage range, as marked on the rear panel.

(2) Set the front panel Power switch to ON.
Remove the locking plate, or plastic cover, of the rear panel voltage selector switches.

(3) Set the multimeter to read 'ohms' and connect between the line and neutral pins of the rear panel mains input plug. Set the mains voltage selection switches to the ranges in Table 8 and verify satisfactory resistance readings.




Mains Voltage Selector Switches Fig.5.1
( LATER MODELS )

TABLE 8

Power (Mains) Input Circuit Resistance

| Voltage Range Selected (See Para. 5.6 or 5.7) | Resistance Reading across Mains Input Plug. |
|---|---|
| 216 - 264V | 106 - 146Ω |
| 188 - 230V | 89 - 129Ω |
| 108 - 132V | 27 - 47Ω |
| 94 - 115V | 23 - 43Ω |

(4) On completion of resistance checks, set the voltage selector switches to the correct positions for the local a.c. supply. Fit the appropriate locking plate, or plastic cover.

## POWER SUPPLY VOLTAGE CHECKS

5.9 (1) Ensure that the preparations in paras. 5.3 to 5.7 have been carried out.

(2) Remove the covers (para.5.2) and connect the a.c. supply.

(3) Set the INPUT switch to channel 'A'
and the Power switch to ON.

(4) Using a multimeter check the d.c. voltages at the following points on the main p.c.b, relative to chassis, as follows:-

Pin 11 +5V ± 0.2V
Pin 14 +4.9V ± 0.3V (for 9921 refer to (6) also)
Pin 17 -5.2V ± 0.2V

Pin 47 +24V ± 1V.

Select INPUT REMOTE and check that Pin 14 reads 0V ± 0.5V

(5) On the 9921, check that Pin 3 on p.c.b. 19-0857 reads -7.5V (± 0.3V) relative to chassis. If necessary adjust R25 on the same p.c.b. for this reading.

(6) On 9921, serial numbers 8010-8059, check the voltage at Pin 14 of the main p.c.b. and verify that the correct resistor values for R25, R29 and R30 are fitted on the p.c.b. 19-0857, depending on the measured voltage, as shown in Table 9. Refer to paras 4.81 to 4.84 for circuit description.

TABLE 9

9921: Pin 14 Voltage/Resistor Values

| Voltage at pin 14 on main p.c.b. | Correct Resistor Value on 19-0857 | | | |
|---|---|---|---|---|
| | R25 | R29 | R30 | Remarks |
| 4.6V - 4.85V | 1.2kΩ | 1.2kΩ | 3.9kΩ | All |
| 4.85 - 5.0V | 1.5kΩ | 1kΩ | 3.9kΩ | ± 2% |
| 5.0V - 5.2V | 1.5kΩ | 680Ω | 3.3kΩ | types. |

## SELF CHECK

5.10 (1) Check that the INPUT switch is not at REMOTE. Set the Power switch to POWER ON and verify that the GATE indicator illuminates.

(2) Set the LF MULTIPLIER switch (if fitted) to the normal (down) position.

(3) Set the following controls:

INPUT switch to 'A'

CHECK/OPERATE/RESET switch to CHECK.

(4) The instrument should now display the 1MHz reference. Refer to Table 10 and operate the GATE TIME switch, verifying that the display agrees with the Table (to a tolerance of + 1 count), and that the 'MHz' and GATE indicators are illuminated. For the 9921 repeat this check with INPUT 'C' selected.

TABLE 10

Self Check Display

| INPUT and GATE TIME Selections | | | Display |
|---|---|---|---|
| INPUT Switch | 'A' | 'C' | |
| GATE TIME Switch | .01 | .02 | 00001.0000 |
| | 0.1 | 0.2 | 0001.00000 |
| | 1 | 2 | 001.000000 |
| | 10 | 20 | 01.0000000 |

(5) Select INPUT 'B' and verify a display of 'all eights' (segment check).

(6) Set the CHECK/OPERATE/RESET switch to OPERATE.

(7) If the LF Multiplier option is fitted, set the LF MULTIPLIER switch to the up position (LF selected). Select INPUT 'A' and verify that the 'Hz' indicator illuminates.

(8) Operate the GATE switch through the four gate time positions and verify the display shown in Table 11.

TABLE 11

Self Check in LF Mode (Option)

| Gate Switch Setting | Display | Tolerance |
|---|---|---|
| .01 | 000000000. | + 1 count |
| 0.1 | 00000000.0 | + 1 count |
| 1 | 0000000.00 | + 5 counts |
| 10 | 000000.000 | + 50 counts |

(9) Set the INPUT switch to REMOTE. If the Remote control option is not fitted the OVERLOW/STANDBY indicator should illuminate, showing that standby mode is in operation. Return the INPUT switch to the 'A' position.

(10) Set the LF Multiplier switch (if fitted) to the down (10Hz · 100MHz) position.

## SENSITIVITY AND AGC CHECK: INPUT 'A'

5.11 Test equipment — Page 5-1 Table 6

| | |
|---|---|
| Signal Generator (10Hz - 105MHz) | Item 4 |
| Oscilloscope | Item 2 |
| BNC 50Ω termination | |

5.12 Procedure

(1) Remove the top cover (para.5.2)

(2) Set the following controls:

(a) LF MULTIPLIER switch (if fitted) to the down position.

(b) INPUT switch to 'A'.

(c) CHECK/OPERATE/RESET switch to OPERATE.

(3) Connect the signal generator to the 'A' input socket using a BNC 50Ω termination.

(4) Refer to the test in Table 12. At each frequency reduce the input level to zero, then slowly increase it until the threshold level for stable counting is reached. Verify that such levels are not higher than those in the Table.

TABLE 12

'A' Channel Sensitivity

| Gate Switch | Input Frequency | Maximum Level for Commencement of Stable Counting. |
|---|---|---|
| 1 | 10Hz | 8mV |
| 1 | 1kHz | 8mV |
| 0.1 | 10MHz | 8mV |
| 0.1 | 32MHz | 8mV |
| 0.1 | 70MHz | 8mV |
| 0.1 | 100MHz | 50mV |

(5) With 100MHz applied at 50mV, set the GATE switch to the 10 secs position and check that the OVERFLOW indicator illuminates after 10 seconds.

(6) Change the signal generator frequency to 10MHz at zero input voltage.

(7) With an oscilloscope, monitor the a.g.c. voltage at Pin 10 of IC22 on the main p.c.b. (see IC 22a on circuit diagram Fig.3).

(8) Slowly increase the input signal level from zero to approximately 100mV r.m.s. and verify that the a.g.c. voltage follows in a positive direction, changing from 0V to 1.1V ± 0.1V.

(9) Disconnect the Oscilloscope.

## SENSITIVITY AND AGC CHECK: INPUT 'B'

5.13 Test equipment — Page 5-1 Table 6

(1) Signal Generators (40MHz - 570MHz). — Item 4

(2) True RMS Millivoltmeter — Item 5

(3) Oscilloscope — Item 2

(4) BNC 'T' Piece

5.14 Procedure

(1) Set the control as follows:

INPUT switch to 'B'
CHECK/OPERATE/RESET switch to OPERATE
GATE switch to 0.1 position.

(2) On the main p.c.b. set potentiometer R68 fully anticlockwise.

(3) Using the millivoltmeter, set the signal generator output level to 8mV at 570MHz.

(4) Disconnect the millivoltmeter and transfer the signal generator output lead to the 'B' input of the unit under test.

(5) Carefully adjust R68 clockwise until the unit just starts to count correctly.

(6) Repeat (3) and (4) for each frequency in Table 13. In each case verify that counting starts cleanly at 8mV, with no tendency to lose or gain counts.

TABLE 13

Sensitivity Check: Input 'B'

| Gate Switch | Input Frequency | Input level for correct counting not to exceed: |
|---|---|---|
| .01 | 400MHz | 8mV |
| 0.1 | 300MHz | 8mV |
| 0.1 | 210MHz | 8mV |
| 1 | 90MHz | 8mV |
| 1 | 38MHz | 8mV |

(7) Set the signal generator frequency to at least 100MHz and set the GATE switch to the 10 secs. position. Press the CHECK/OPERATE/RESET switch to RESET and release. Check that the display resets to zero and that after 10 seconds the OVERFLOW indicator illuminates.

(8) Set the signal generator to 40MHz and zero input voltage.

(9) With an oscilloscope, monitor the a.g.c. voltage on pin 10 of IC29 on the main p.c.b. (see Fig.3, IC 29b).

(10) Slowly increase the input signal level from zero to approximately 100mV r.m.s. and verify that the a.g.c. voltage changes in a positive direction from approximately -3V to +3V.

(11) Disconnect the oscilloscope.

## OFF CHIP COUNTER CHECK

5.15 Test Equipment — Page 5-1 Table 6

| | |
|---|---|
| VHF Signal Generator | Item 4 |

5.16 Procedure

(1) Set the controls as follows:

INPUT switch to 'A'
CHECK/OPERATE/RESET switch to OPERATE
GATE switch to 0.01s

(2) Apply 40MHz at 100mV r.m.s. to the 'A' input socket.

(3) Using the signal generator fine tune control, slowly adjust the frequency and check that all numerals 0-9 are displayed on the last two (least significant) digits.

(4) Check that carry from each of the two digits occurs on the 9 to 0 transition.

(5) Disconnect the test equipment

## Overload Indicator Check

5.17 This facility can be checked using a v.h.f. generator capable of supplying up to 8.5V r.m.s. output at 100MHz, connected to the 'B' input. The OVERLOAD INDICATOR should illuminate at an input voltage in the range 5.5V r.m.s. to 8.5V r.m.s.

## FREQUENCY STANDARD CHECKS

5.18 Test Equipment — Page 5-1 Table 6

| | |
|---|---|
| Oscilloscope | Item 2 |
| External IMHz Frequency Standard | Item 3 |

5.19 Frequency Standard Input/Output Check

(1) Set the oscilloscope controls to 'External Trigger' and '100ns/cm' timebase, and connect the probe to the 1MHz O/P socket on the rear panel of the counter (unterminated).

(2) With the counter switched on, observe the approximately 1:4 rectangular output waveform at 1MHz, and verify 3V p-p amplitude.

(3) Trigger the oscilloscope with the 1MHz external frequency standard, at approximately 1V r.m.s., and observe the trace moving slowly across.

(4) Now connect an output from the external standard to the counter EXT STD I/P socket and check that the trace and trace locks and the front panel EXTERNAL STANDARD indicator illuminates.

(5) Disconnect the external standard from the counter.

Internal Frequency Standard Calibration

5.20 The 'cycle drift' method of frequency calibration, described below, is suitable for oscillators which have temperature stability characteristics up to 1 part in $10^8$. With higher stability oscillators, such as the Racal 9421 and 9442, specialised equipment such as the Tracor Frequency Difference Meter Type 527A is advised if the optimum calibration is to be achieved.

5.21 (1) The instrument must be switched on at least one hour before commencing the calibration of a temperature-controlled frequency standard.

(2) Set up the equipment as in 5.19 (1) and (3).

(3) Observe the oscilloscope display and check the amount of drift occurring in 10 seconds:

10 division in 10 seconds = 1 part in $10^7$
1 division in 10 seconds = 1 part in $10^8$

(4) If necessary, adjust the frequency standard trimmer via the hole in the rear panel, to obtain a stationary trace. Use a screwdriver of low thermal capacity. The 9421 (option 04B) has two adjustments, coarse and fine.

## CALIBRATION: INPUT 'C' (9921 ONLY)

NOTE: The following tests assume that p.c.b's 19-0857 and 19-0871 are serviceable. Detailed test procedures for these boards are given in the supplementary calibration procedures commencing at para. 5.24.

5.22 Test Equipment — Para. 5-1 Table 6

| | |
|---|---|
| UHF Signal Generator (1GHz - 3GHz) | Item 2 |
| Oscilloscope with x 10 probe | Item 4 |

5.23 Sweep and Lock Check

(1) Switch power off and remove covers (see para. 5.2).

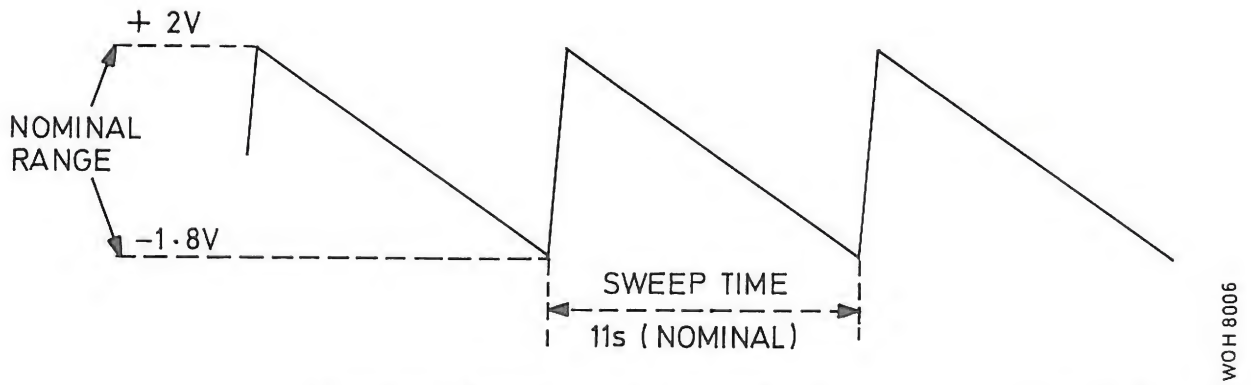
(2) Partly detach p.c.b. 19-0857 to gain access to component side of 3GHz assemblies. See Chapter 6 para. 6.6.

(3) Set the controls:

POWER ON
GATE switch to channel 'C'.

(4) Connect the oscilloscope using x 10 probe to pin 2 of p.c.b. 19-0856 (Top Loop and Sampler). Do not apply an external signal.

(5) Check the top loop sweep by verifying that the oscilloscope display sweeps linearly from +2V to -1.8V approximately, (Fig. 5.2 below) with a sweep time of 11 seconds ± 1.0 seconds. If necessary adjust R3 on the p.c.b. to set the correct sweep time.




Sweep Waveform Diagram Fig.5.2

(6) Transfer the oscilloscope probe to pin 10 p.c.b. 19-0857 (2nd Loop and Output Processor) and verify the same sweep display as in (4), thus checking that the 2nd loop tracks the top loop.

(7) Change oscilloscope to x 1 probe tip, and monitor test point TP6 on p.c.b. 19-0857 (AGC input).

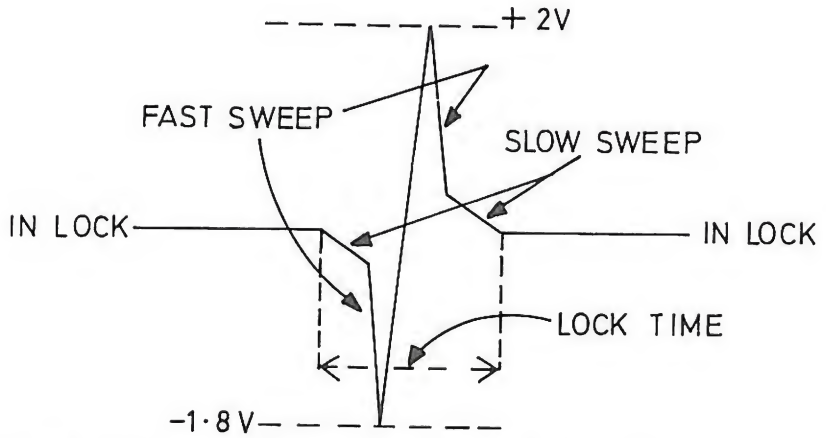
(8) Observe the 50kHz transient and verify a p-p amplitude not exceeding 10mV.

(9) Set the signal generator to 300MHz at -13dBm, and connect to the 'C' input socket.

(10) Check that the display is stable and correct.

(11) Refit the x 10 probe to the oscilloscope and monitor pin 2 of Top Loop and Sampler p.c.b. 19-0856.

(12) Put the system out of lock by a sharp change of signal generator frequency and observe the waveform of the sweep speed-up circuit (Fig. 5.3 below). Check that the time to achieve lock does not exceed 2 seconds.




Sweep Speed-up and Lock Waveform Diagram Fig.5.3

(13) Increase the input level to 0dBm. Check at TP7 on 19-0857 for 300mV p-p (a.g.c. output level). If necessary adjust R59 on the same p.c.b. for this reading.

(14) Increase the signal generator level to +13dBm and verify correct and steady counting at 300MHz.

(15) At frequencies of 1GHz and 3GHz check for correct and steady counting at +13dBm input. In each case reduce the level to -13dBm and verify that stable counting is maintained.

(16) Gradually reduce the input level until the inhibit operates, causing the display to reset to zeros. This should occur at a level below -19dBm.

## SUPPLEMENTARY CALIBRATION PROCEDURES (9921)

### INTRODUCTION

5.24 The following paragraphs contain instructions for the independent testing and setting-up of the p.c.b. Assemblies in the 3GHz section of the 9921.

5.25 The tests can be made with the p.c.b. Assemblies mounted in a serviceable instrument using normal power supplies, provided that certain disconnections are made, as instructed. The tests must be made in the sequence given with satisfactory completion of each test before proceeding to the next.

**CAUTION**

ALWAYS SWITCH OFF THE POWER SUPPLY BEFORE DISCONNECTING OR RE-CONNECTING LINKS, THE SIGNAL GENERATOR OR OTHER TEST EQUIPMENT. THIS INSTRUCTION WILL NOT BE REPEATED IN THE TEST PROCEDURES.

### TOP LOOP AND SAMPLER ASSEMBLY 19-0356

5.26 Test Equipment — Page 5-1 Table 6

| | |
|---|---|
| Multimeter | Item 1 |
| Oscilloscope with x 10 probe (dual trace) | Item 2 |
| Universal Counter Timer | Item 6 |
| Signal Generator 1...HF (1MHz - 30MHz). | Item 4 |
| Signal Generator 2...UHF (300MHz - 3GHz). | Item 4 |
| Millivoltmeter (True RMS) | Item 5 |

Coaxial cable BNC to open end with 56Ω resistor across open end.
Coaxial cable BNC to open end, unterminated.

NOTE: Access to the component side of the assemblies in the 3GHz section is obtained by placing the instrument bottom side uppermost and partly detaching the 2nd Loop and Output Processor p.c.b. See Chapter 6, para. 6.6.

#### Power Check

5.27 (1) Remove covers (para. 5.2.) and switch on the a.c. supply.

(2) Using the multimeter check the following nominal voltages on p.c.b. 19-0856:

Pin 20 ...+5V Pin 22 ...-7.5V.
Pin 21 ...0V Pin 19 ...+24V.

## Disconnections

5.28 Switch off, and disconnect, the leads at pins 1 to 6 inclusive on the Compensator p.c.b. 19-0871. Instructions for other disconnections will be given in the procedures.

## VCO Setting-Up Procedure (Fig.7)

5.29 (1) Using a multimeter check the d.c. voltages at the following test points on 19-0856.

TP8 (VCO supply) .... -6.6V ± 0.35V
TP13 (+11V supply) .....+11.3V ± 0.7V
TP14 (VCO setting up +ve) ... +2V ± 0.2V
TP15 (VCO setting up -ve) ... -1.8V ± 0.2V

(2) On 19-0856 disconnect pin 1 from pin 2 (link LK3 on Fig.7) thus breaking the VCO tuning control line.

(3) On 19-0856 connect pin 1 to TP15 thus applying -1.8V to the VCO control line, to hold the oscillator at its lowest frequency (circuit diagram Fig.7)

(4) Using an oscilloscope with x 10 probe verify that the oscillator output level at TP9 is 1.8V p-p approximately.

(5) Connect a frequency counter via x 10 probe to TP10 (VCO output) and verify a frequency of 19MHz ± 100kHz. If necessary adjust the core of L12 to set the frequency to 19MHz.

(6) Disconnect pin 1 from TP15 and connect pin 1 to TP14, thus applying +2V to the VCO control line to obtain the highest oscillator frequency.

(7) Repeat operation (5) to verify a frequency of 21MHz ± 0.6MHz. Do not adjust L12.

## Filter Check

5.30 (1) Disconnect pin 7 from pin 8 (link LK1 on circuit Fig. 6)
Maintain the link between Pin 1 and TP14.

(2) Connect signal generator 1 to pin 8 (line) and pin 9 (0V) using coaxial lead terminated with 50 ohms.

(3) Set the signal generator level to 1V p-p measured at pin 8.

(4) Connect the oscilloscope to TP11 (filter output Q21 Fig.7) using the probes listed in Table 14 below. Check the filter response in accordance with the Table.

TABLE 14

Filter Response Check : 19-0856

| Input Frequency | Amplitude at TP11 | Probe used |
|---|---|---|
| 10MHz | Not less than 700mVp-p | x 10 |
| 13-30MHz | Not greater than 5mVp-p | x 1 with h.f. probe tip. |

(5) Disconnect the signal generator and oscilloscope.

(6) Re-connect pin 8 to pin 7 (link LK1).

5.31 Dual Sampler Check (19-0752 and 19-0856)

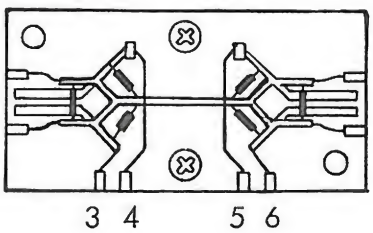
NOTE: The sub-Assembly 19-0752 is mounted on the track side of 19-0856. If faulty it should be returned to the manufacturer for repair.

(1) Unsolder the coaxial lead from pin 15 of 19-0856 (circuit Fig. 7).

(2) Connect signal generator 1 to pin 15 and pin 16 (0V) on 19-0856 using unterminated 'open end' coaxial lead.

(3) Set the signal generator to 20MHz and a level of 300mV p-p, measured at pin 15.

(4) Using an oscilloscope with x10 probe, check the d.c. voltages on pads 3,4, 5 and 6 on the Dual Sampler Sub-Assembly (Fig. 5.4).




Sampler Sub-Assembly Test Points Fig. 5.4

Pin 3 and Pin 6: approximately -0.9V
Pin 4 and Pin 5: approximately +0.9V
} relative to 0V.

(5) Maintain the 20MHz 300mV signal generator input at pin 15. Maintain the link between Pin 1 and TP14.

5.32 Sweep Speed-up Circuit: 19-0856

(1) With signal generator 1 connected as in (5) above, connect signal generator 2 to the 'C' front panel input socket and apply a signal of 300MHz at -13dBm.

(2) Using oscilloscope(s), simultaneously monitor pin 12 and TP12, using a x 10 probe on TP12. (Circuit Fig. 7).

(3) The beat frequency observed at TP12 can now be varied by slightly adjusting the frequency of signal generator 2. Adjust for a beat frequency ('f') of less than 1MHz and verify that pin 2 is at logic level '0'.

(4) Increase the beat frequency 'f' until pin 12 goes to logic level '1' and check that 'f' is approximately 1MHz.

(5) Continue to adjust the frequency of signal generator 2 in the same direction as in (4) such that the beat frequency 'f' increases from approximately 1MHz, passes through a maximum value and then returns to approximately 1MHz. Check that Pin 12 remains at logic level '1' while the beat frequency is above 1MHz.

(6) Set the level of signal generator 2 to -50dBm.

(7) Disconnect pin 1 from TP14. Close the loop linking pin 1 to pin 2 (link LK3).

(8) Check that there are no connections to pins 1 to 6 of the Compensator p.c.b. 19-0871 but that pins 7, 8 and 9 are connected to 22, 20 and 21 of 19-0856.

(9) On the Compensator p.c.b. 19-0871 link pins 6 and 2 to 0V, and pin 3 to +5V (at pin 8).

(10) On 19-0871 monitor IC4 pin 10 and verify logic level '0'. Short circuit pin 5 on the p.c.b. to 0V and verify that IC4 pin 10 changes to logic '1'.

(11) Remove short circuit from pin 5 and monitor TP2 for a rectangular waveform with a period of 25µs (±5µs), and amplitude between TTL levels.

(12) Using a 1:1 probe, observe a sawtooth waveform on pin 1, ramping from -0.25V to 0.25V. Expand the trace and verify a step size of approximately 2mV. Check that there are no missing steps.

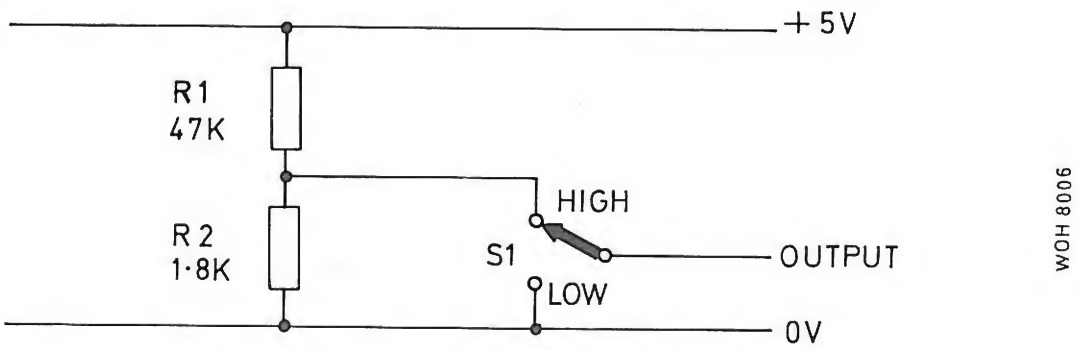
(13) Remove all links fitted during operations (9) and (10) and reconnect the leads between p.c.b.'s 19-0871 and 19-0856, as follows:

| 19-0871 | 19-0856 |
|---|---|
| Pin 1 | Pin 13 |
| 2 | 14 |
| 3 | 5 |
| 4 | 11 |
| 5 | 12 |
| 6 | 10 |

(14) Turn R8, on 19-0356, fully clockwise.

(15) Connect an oscilloscope with x 10 probe to pin 2 of 19-0856. Observe an approximately linear sweep from approximately +2V to approximately -1.8V before resetting.

(16) Make up the test circuit in Fig. 5.5, and connect the output of the switch to pin 6 of the dual FET Q7 (see Fig. 5 for location).




Sweep Test Switch Fig.5.5

(17) Set the switch in the 'Lo' position and adjust R8 to give a sweep time of 11 seconds ± 1 second .

(18) Set the switch to the 'Hi' position and note that the sweep speed increases, but is automatically corrected to a time of 11 seconds (± 1 second) after the next sweep reset.

(19) Return the switch to the 'Lo' position and check that the sweep ramps upwards and that the sweep rate is corrected to 11 seconds (± 1 second) after the integrator output reaches approximately 2.7V.

(20) Disconnect the test switch circuits, connected in (16) and adjust R8 for a sweep time of 11 seconds, ± 1 second (The adjustment will have no effect until after the next sweep reset.).

(21) Set signal generator 2 to a frequency of 300MHz at 0dBm. Monitor the integrator output (pin 4) and verify a steady d.c. level, which indicates that the loop is in lock (not sweeping).

(22) Disconnect all test equipment from the board and reconnect the coaxial lead to pin 15, disconnected in (1).

## 2nd LOOP AND OUTPUT PROCESSOR ASSEMBLY 19-0857 (Figs 10 & 11)

### Preliminary

5.33 (1) Refer to the CAUTION and NOTE in para. 5.25

(2) The test on p.c.b. 19-0856 and 19-0752 and 19-0871 should have been satisfactorily completed.

5.34 Test Equipment — Page 5-1 Table 6

| | |
|---|---|
| Multimeter | Item 1 |
| H.F. Signal Generator (1 - 30MHz). | Item 4 |
| Oscilloscope with x 10 probe | Item 2 |
| Universal Counter Timer (Ratio Counter) | Item 6 |
| Coaxial lead (50Ω) BNC to 'open end' | Item 7 |
| Coaxial lead (50Ω) BNC to 'open end', terminated with 50Ω | Item 7 |
| Terminating network (see para. 5.37) | |

5.35 Power Check

(1) With power switched on check the following voltages on 19-0857.

Pin 4 ..... 0V

Pin 5 ..... -10V

Pin 7 ..... +5V

Pin 3 (-7.5V regulator)..... -7.5V ± 0.33V

TP2 (VCO supply) ..... -6.6V ± 0.35V

5.36 Phase Locked Loop: 19-0857

(1) Unsolder the coaxial connection from pins 8 and 9. (Circuit diagram Fig.10).

(2) If the p.c.b. has not previously been used check that link LK1 is fitted between pins 10 and 11 (Output from IC5 in Fig. 11).

(3) Using the BNC to 'open end' (unterminated) coaxial lead connect the signal generator to pin 8 and pin 9 (0V) on 19-0857. Set the signal generator to 19MHz and 300mV peak-to-peak at pin 8.

(4) Using oscilloscope with x 10 probe check that the oscillator output level at TP3 is approximately 1.8V peak-to-peak.

(5) Verify that the loop is in lock by checking the d.c. voltage on pin 10 (LK1, integrator output). The required level is -1.8V ± 0.2V. If necessary adjust L7 to obtain this voltage.

(6) Connect the Ratio Counter input sockets to Pin 8 (higher frequency) and TP1 (lower frequency) and check that division by 400 is obtained.

(7)q Repeat operation (6) but between TP4 (IC1a input) and TP5 (IC4 input) checking for division by 399.

(8) Repeat the ratio check between TP1 and TP 5 with the ratio counter set to $n = 10^5$. Verify a readout of 100 000 ± 1 count.

(9) Check the tracking of the loop by slowly shifting the signal generator frequency from 19MHz through to 21MHz. The d.c. level on pin 10 should shift in sympathy from -1.8V to +2V approximately.

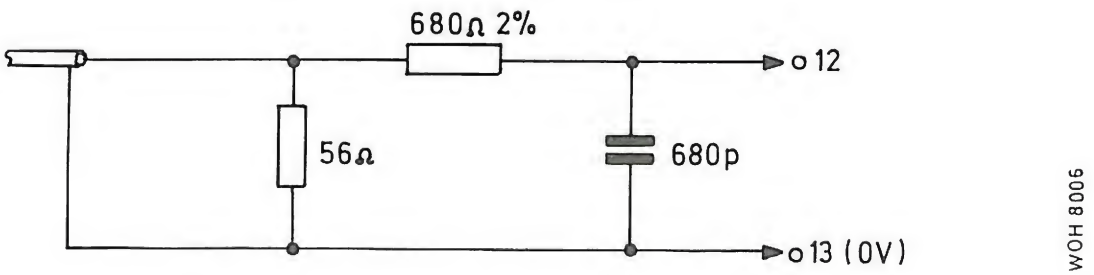
(10) Disconnect the signal generator from pins 8 and 9.

(11) Resolder the coaxial connection to pins 8 and 9 (disconnected in (1) ).

5.37 Output Processor Check: 19-0857

(1) Unsolder the coaxial lead from pins 12 and 13. Circuit Fig.11).

(2) Connect the Signal Generator to pins 12 and 13 (0V) using 50Ω coaxial cable terminated with a network as in Fig. 5.6.




Terminating Network Fig.5.6

(3) Set the signal level to 1V peak-to-peak at junction of 56Ω/680Ω

(4) Connect the oscilloscope to TP6 using x 1 probe and probe tip.

(5) Check the filter response at the following frequencies:

| Frequency | Amplitude at TP6 (Peak-to-Peak) |
|---|---|
| 7.5MHz | 700mV ± 200mV |
| 13-30MHz | Less than 2mV |

(6) Set the signal generator frequency to 1MHz.

(7) Transfer the oscilloscope to TP7 and verify an AGC output of 300mV ± 50mV p-p. If necessary adjust R59 for this output.

(8) Reduce the input level until the level at TP7 just falls below the AGC level set in (7). Check that the input level is 30mV ± 5mV p-p. Check that the inhibit line (TP9) is at logic level '1' .

(9) Reduce the input level further until TP9 changes to logic level '0'. Note the input level which should be less than 30mV.

(10) Set the signal generator frequency to 7.5MHz and the level to above 30mV, then repeat operation (8).

(11) Set the signal generator level to 60mV.

(12) Check the frequency doubler by connecting the Universal Counter (Ratio mode) to Pin 15 (higher frequency) and IC11 pin 6 (lower frequency). Using $n = 10^5$ range, verify a ratio readout of 200,000 ± 1 count.

(13) With the Universal Counter on Frequency mode, verify that the frequency display remains unchanged as the signal generator level is increased to 2V p-p.

(14) Disconnect test equipment.

(15) Reconnect the coaxial cable to pins 12 and 13, disconnected in (1).

# CHAPTER 6

# DISMANTLING AND REASSEMBLY

## INTRODUCTION

6.1 When unsoldering connecting leads or components a suitable low-wattage soldering iron should be used, and care should be taken to apply the minimum of heat for the purpose, especially when working close to the printed circuit track.

CAUTION: ENSURE THAT THE A.C. SUPPLY IS COMPLETELY DISCONNECTED BEFORE COMMENCING ANY DISMANTLING OR FITTING.

## REMOVAL OF MAIN PCB

6.2 This p.c.b. has excellent accessibility and all servicing can be carried out with the board in situ. In the very unlikely event of removal being necessary proceed as follows:-

(1) Release the strap securing the two electrolytic capacitors to the side panel.

(2) Unsolder the connections to:-

(a) Three regulator IC's
(b) Four wires of the d.c. supply
(c) The frequency standard connections
(d) Connections to the 3GHz section and LF Multiplier option (if fitted). Unplug the Remote and BCD option board (if fitted).
(e) The resistor connected to the 'A' channel input plug.
(f) Release the display assembly from the front panel. (See para. 6.3 operations (1) to (3).

(3) Unscrew the 3 screws and two pillars on the underside of the main p.c.b. and withdraw the whole assembly, with large capacitors and display assembly attached.

(4) When the two assemblies are removed, carefully unsolder the 33-way flexible connector from the main p.c.b. and detach the display assembly.

(5) Unsolder the two large electrolytic capacitors, as they are not supplied with a replacement main p.c.b., unless specified. Similarly, the regulator IC's on the side panel are listed in the chassis assembly parts list.

(6) Reassembly is the reverse of the dismantling procedure.

## CHANGING A DISPLAY LED INDICATOR

6.3 This procedure involves partial removal of the display assembly; proceed as follows:-

(1) Unclip any wiring loom which is secured to the display assembly.

(2) Remove the two screws which secure the display assembly to the rear of the front panel.

(3) Carefully ease the display assembly rearwards and then fold it face downwards.

(4) Unsolder the l.e.d. pins from the track and withdraw the l.e.d.

(5) Fit the new l.e.d.; solder in; then refit the display assembly, following the above instructions in reverse order.

## REMOVAL OF DISPLAY ASSEMBLY

6.4 Do not remove this assembly, unless it is unavoidable , because of the effort involved in disconnecting the 33-way flexible connector. For removal follow the instructions in para. 6.3 (1) to (3) and then very carefully unsolder the 33-way connector. Should it be necessary to replace this loom, the part number is 25-6027.

## 3GHz SECTION ASSEMBLIES

### Location

6.5 These are located on the right hand side of the instrument, the Top Loop and Sampler (19-0856) is the upper board. The 2nd Loop and Output Processor (19-0857) is the lower. The sub-Assemblies 19-0852 and 19-0871 are attached to the Top Loop and Sampler PCB.

### Access for Servicing

6.6 To gain access to the component sides of the 3GHz assemblies it is necessary to 'hinge' the 2nd Loop and Output Processor Assembly upwards (endwise) and rest it on a sheet of card or thick paper to prevent short circuits to chassis. This can be done by placing the instrument bottom uppermost and removing the screws from the p.c.b. Take care not to strain the wiring when 'hingeing'.

## REMOVAL OF FREQUENCY STANDARD

6.7 The ovened frequency standards are held by two screws on the rear panel. First unsolder the leads from the unit base then remove the screws while supporting the unit.

6.8 When fitting a 9421 unit check that pins 5 and 6 are linked on the base.

## FITTING REMOTE CONTROL AND BCD OUTPUT ASSEMBLY 19-0859 (OPTION 02)

### Option Kit

6.9 The kit is supplied under Part No. 11-1242 and contains the following items:-

(a) PCB Assembly 19-0859 complete with cableforms having 14-way and 50-way connectors attached.

(b) Bracket assembly with 4 screws (M3, 8lg) and washers.

### Fitting

6.10 (1) Remove the 'Remote Control' and 'BCD Output' blanking plates from the rear panel. Retain the screws and washers.

(2) Take the p.c.b. assembly: remove the wire clips from the cable loom connectors, and feed the cable and connectors from inside the instrument, through the gap between the frequency standard unit and the mains transformer, so that the two connectors emerge through their correct apertures in the rear panel.

(3) Refit the wire clips and secure the connectors to the rear panel, using the screws and washers removed in (1).

(4) Inside the instrument remove and retain the screw and washer from the centre of the crossmember.

(5) Position the p.c.b. assembly vertically behind the crossmember and press the p.c.b. edge connector into the socket on the main p.c.b.

(6) Secure the p.c.b. bracket to the crossmember, using the fixings removed in (4) and the two screws and washers supplied.

## FITTING LF MULTIPLIER ASSEMBLY (OPTION 09)

### Option Kit

6.11 The kit consists essentially of:-

(a) PCB Assembly 19-0797
(b) Toggle switch Part No. 23-4065
(c) Two spacers and M3 x 12 screws with washers.

### Location

6.12 Looking at the front of the instrument the p.c.b. is to be mounted on the left hand face of the vertical bracket above the main p.c.b. just forward of the crossmember. Two captive nuts are fitted for attachment.

Fitting

6.13 (1) Remove the rubber plug from the 'LF Multiplier' switch position on the front panel and fit the toggle switch in the aperture.

(2) Fit the LF Multiplier p.c.b. to the bracket, fitting the spacers between board and bracket, and securing with the M3 screws and washers supplied.

(3) Pass the p.c.b. wiring under the crossmember and solder to pins31 to 35 on the main p.c.b. These pins are identified on component layout diagram Fig. 2. For wiring schedule see Table 15 below, or refer to circuit Fig. 3. Dress wires neatly and strap together.

(4) Connect toggle switch centre tag to pin 23 and the lower tag to pin 26 on the main p.c.b. These pins are located just beneath the 33-way flexible connector, but are accessible. See component layout Fig.2.

TABLE 15

LF Multiplier Connections (Option 09)

| Wire No. | Colour | Length | From | To (Main PCB) |
|---|---|---|---|---|
| 1 | White | 150mm | Toggle SW | PIN 23 |
| 2 | White | 150mm | Toggle SW | PIN 26 |
| 3 | White | 170mm | 19-0797 PIN 3 | PIN 31 |
| 4 | White-Black | 130mm | PIN 2 | PIN 33 |
| 5 | White-Yellow | 180mm | PIN 5 | PIN 32 |
| 6 | White-Violet | 140mm | PIN 1 | PIN 35 |
| 7 | White-Red-Blue | 190mm | PIN 4 | PIN 34 |

# SECTION 3

# PARTS LISTS

# CIRCUIT DIAGRAMS

# AND

# COMPONENT LAYOUTS

## ORDERING OF SPARE PARTS

1. To be assured of satisfactory service when ordering replacement parts, the customer is requested to include the following information.

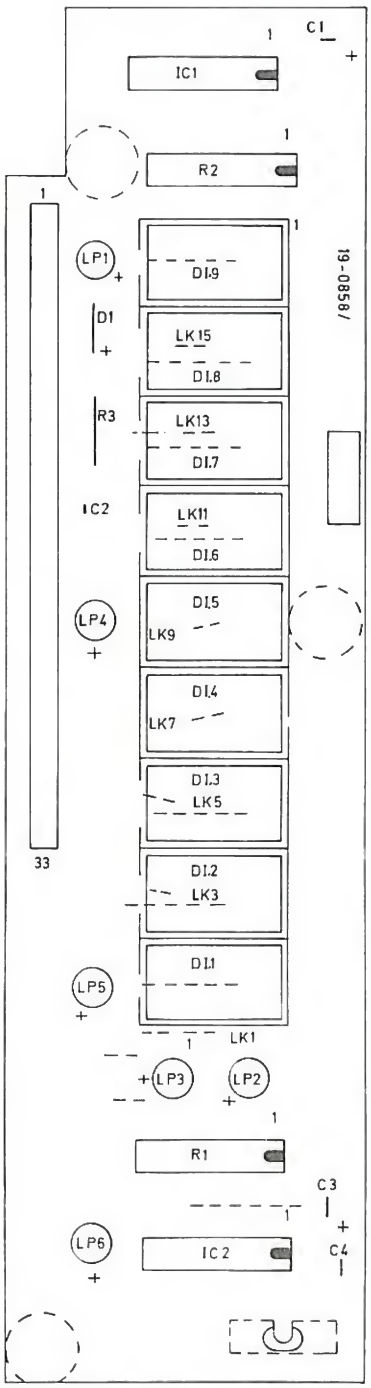
   (a) Instrument type and serial number.

   (b) The type reference of the Assembly in which the particular items is located (for example, '19-0834').

   (c) The Racal Part number and circuit reference of each item being ordered.

   It should be noted that a minimum charge of £5 sterling is applicable to all U.K. orders.

NOTES 1 COMPONENTS ARE PREFIXED '1' IN CIRCUIT DIAGRAM (FIG. 4)




RACAL

| WOH 8006 | 19-0858 |
|---|---|
| 1 | |

# Component Layout : Display Assembly 19-0858

Fig. 1

# PARTS LISTS COMPONENT LAYOUTS AND CIRCUIT DIAGRAMS

## CONTENTS


9918 and 9921

Component Layout: Display Assembly 19-0853. Fig. 1
Parts List for Display Assembly see Parts List 2b.

Parts List 1: Chassis, Front and Rear Panel Assemblies

Parts List 2a and 2b: Main PCB Assembly
Component Layout: Main PCB Assembly 19-0855 Fig. 2
Overall Circuit 9918 & 9921 (Part 1) Fig. 3
Overall Circuit 9918 & 9921 (Part 2) Fig. 4

---

9921 Only

Parts List 3: 19-0856
Component Layout: Top Loop and Sampler Assembly 19-0856 Fig. 5
Circuit: Top Loop and Sampler Assembly 19-0856 (Part 1) Fig. 6
Circuit: Top Loop and Sampler Assembly 19-0856 (Part 2) Fig. 7

Parts List 4: 19-0871
Component Layout and Circuit: Digital Offset Compensation Assembly 19-0871 Fig. 8

Parts List 5: 19-0857
Component Layout: 2nd Loop and Output Processor Assembly 19-0857 Fig. 9
Circuit: 2nd Loop and Output Processor Assembly 19-0857 (Part 1) Fig. 10
Circuit: 2nd Loop and Output Processor Assembly 19-0857 (Part 2) Fig. 11

---

9918 and 9921 Options

Parts List 6: 19-0834
Circuit and Layout: Oscillator Assembly 19-0834 (Option 04C) Fig. 12

Parts List 7: 19-0797
Circuit and Layout: LF Multiplier Assembly 19-0797 (Option 09) Fig. 13

Parts List 8: 19-0859
Component Layout: Remote Control and BCD Output Assembly 19-0859 Fig. 14
Circuit: Remote Control and BCD Output Assembly 19-0859 (Option 02) Fig. 15

## PARTS LIST

### CHASSIS, FRONT AND REAR PANELS (Figs. 3 and 4)

| Part No. | Description | Component Reference |
|---|---|---|
| **FRONT PANEL ASSEMBLY COMPONENTS** | | |
| 23-4044 | Switch, toggle, SP-DT | S50 |
| 23-4090 | Switch, toggle, DP-ST, 3A, 250V | S54 |
| NOTE: For GATE and INPUT switches refer to Main PCB Parts List. | | |
| 23-4065 | Switch toggle, SP-DT, on-on (Option 09) | S51 |
| 23-3030 | Sockets, BNC, 'A' and 'B' inputs | SK50, SK51 |
| 10-2449 | Cable Assembly, with 'C' input socket for 9921 | |
| 26-5003 | Indicator, l.e.d., red (HP5082-4850) | LP50 |
| **REAR PANEL ASSEMBLY COMPONENTS** | | |
| 17-4049 | Transformer, mains | T50 |
| 22-1650 | Bridge rectifier, 200V, 2A (VS248) | D50 |
| 23-0043 | Fuselink (118V/265V) 125mA antisurge | FS50 |
| 23-0031 | Fuselink (94V/132V) 250mA antisurge | FS50 |
| 23-0044 | Fuseholder for FS50 | |
| 23-3005 | Socket BNC. STD input and output | SK52, 53 |
| 23-3194 | Power Input (Mains) plug and filter | PL50 |
| | Frequency Standard options 04A and 04B, see Tech. Spec. | |
| 19-0834 | Frequency Standard PCB option 04C, see Parts List 2. | |
| **CHASSIS ASSEMBLY COMPONENTS (including side panels)** | | |
| 20-2101 | Resistor, carbon film, $\frac{1}{4}$W, 5% 100Ω | R300 |
| 21-4528 | Capacitor, polyester, 400V, 10%, 47nF | C100 |
| 21-0575 | Capacitor, electrolytic, 16V, 4700μF | C101 |
| 21-0576 | Capacitor, electrolytic, 25V, 2200μF | C102 |
| 22-4222 | Regulator +5V | IC50, IC51 |
| 22-4223 | Regulator -5V | IC52 |

## PARTS LIST FOR FIG. 3 & FIG. 4

### MAIN PCB ASSEMBLY 19-0855

| Part No. | Description | Rat | Tol % | Value | Component Reference |
|---|---|---|---|---|---|
| | **Resistors** | **W** | | **Ω** | |
| 20-1514 | Carbon film | 0.1 | 5 | 100 | R93 |
| 20-1515 | Carbon film | 0.1 | 5 | 180 | R146 |
| 20-1516 | Carbon film | 0.1 | 5 | 220 | R12, 19, 52 |
| 20-1517 | Carbon film | 0.1 | 5 | 330 | R18, 20 |
| 20-1519 | Carbon film | 0.1 | 5 | 68 | R29 |
| 20-1521 | Carbon film | 0.1 | 5 | 1k | R5, 77, 132 |
| 20-1523 | Carbon film | 0.1 | 5 | 120 | R25, 53 |
| 20-1528 | Carbon film | 0.1 | 5 | 2.2k | R54, 152 |
| 20-1561 | Carbon film | 0.1 | 5 | 1M | R2 |
| 20-1563 | Carbon film | 0.1 | 5 | 22k | R62, 69 |
| 20-1527 | Carbon film | 0.1 | 5 | 270 | R31, 32, 65, 33 |
| 20-1532 | Carbon film | 0.1 | 5 | 470 | R21, 51, 59, 71, 73 |
| 20-1533 | Carbon film | 0.1 | 5 | 5.6k | R46 |
| 20-1538 | Carbon film | 0.1 | 5 | 10k | R24, 28, 61, 101 110, 111 |
| 20-1541 | Carbon film | 0.1 | 5 | 1.8k | R50 |
| 20-1542 | Carbon film | 0.1 | 5 | 4.7k | R15, 147, 148 |
| 20-1544 | Carbon film | 0.1 | 5 | 1.2k | R48 |
| 20-1545 | Carbon film | 0.1 | 5 | 1.5k | R76 |
| 20-1554 | Carbon film | 0.1 | 5 | 680 | R81 |
| 20-2101 | Carbon film | ¼ | 5 | 100 | R64, 91, 105, 106, 126 |
| 20-2102 | Carbon film | ¼ | 5 | 1k | R22, 26, 108, 120, 130, 149, 151 |
| 20-2103 | Carbon film | ¼ | 5 | 10k | R17, 55, 57, 74, 75, 98, 99, 107, 114 124, 129, 131, 135, 136 |
| 20-2104 | Carbon film | ¼ | 5 | 100k | R16 |
| 20-2105 | Carbon film | ¼ | 5 | 1M | R36 |
| 20-2106 | Carbon film | ¼ | 10 | 10M | R40 |
| 20-2120 | Carbon film | ¼ | 5 | 12 | R9 |
| 20-2122 | Carbon film | ¼ | 5 | 1.2k | R37, 150 |
| 20-2123 | Carbon film | ¼ | 5 | 12k | R39 |
| 20-2150 | Carbon film | ¼ | 5 | 15 | R112, 113 |
| 20-2152 | Carbon film | ¼ | 5 | 1.5k | R56, 86, 95, 123 |
| 20-2181 | Carbon film | ¼ | 5 | 180 | R88 |
| 20-2182 | Carbon film | ¼ | 5 | 1.8k | R10, 11, 13, 94 |
| 20-2183 | Carbon film | ¼ | 5 | 18k | R144 |
| 20-2184 | Carbon film | ¼ | 5 | 180k | R47 |
| 20-2220 | Carbon film | ¼ | 5 | 22 | R66 |
| 20-2222 | Carbon film | ¼ | 5 | 2.2k | R4, 63, 97, 102, 104, 125, 126, 154 |
| 20-2223 | Carbon film | ¼ | 5 | 22k | R127 |
| 20-2271 | Carbon film | ¼ | 5 | 270 | R34, 41, 89 |
| 20-2272 | Carbon film | ¼ | 5 | 2.7k | R79, 85, 133 |
| 20-2331 | Carbon film | ¼ | 5 | 330 | R7, 43, 45, 92, 116, 117, 118, 121, 134, 137, 138, 140, 142, 145, 153 |
| 20-2332 | Carbon film | ¼ | 5 | 3.3k | R80, 84, 103, 115, 119, 143 |
| 20-2390 | Carbon film | ¼ | 5 | 39 | R44 |
| 20-2471 | Carbon film | ¼ | 5 | 470 | R6, 23, 70, 72, 139 |
| 20-2472 | Carbon film | ¼ | 5 | 4.7k | R109, 141 |
| 20-2474 | Carbon film | ¼ | 5 | 470k | R30 |
| 20-2560 | Carbon film | ¼ | 5 | 56 | R33 |
| 20-2562 | Carbon film | ¼ | 5 | 5.6k | R42 |
| 20-2681 | Carbon film | ¼ | 5 | 680 | R78, 82, 87 |
| 20-2683 | Carbon film | ¼ | 5 | 68k | R60 |
| 20-2821 | Carbon film | ¼ | 5 | 820 | R90 |

| Part No. | Description | Rat | Tol % | Value | Component Reference |
|---|---|---|---|---|---|
| | | **W** | | **Ω** | |
| 20-3103 | Metal Oxide | ½ | 5 | 10k | R35 |
| 20-3390 | Metal Oxide | ½ | 5 | 39 | R38 |
| 20-4658 | Metal Oxide | 1 | 5 | 100k | R3 |
| 20-7034 | Variable, cermet | | 10 | 2.2k | R68 |
| | **Resistor Arrays** | | | | |
| 20-5502 | DIL (13 x 1k) | | | | R122 |
| 20-5503 | DIL (13 x 10k) | | | | R100 |
| 20-5507 | DIL (13 x 3.3k) | | | | R96 |
| 20-5509 | DIL (8 x 470) | | | | R27 |
| | **Capacitors** | **V** | | **F** | |
| 21-0648 | Electrolytic | 40 | -10+50 | 470µ | C83 |
| 21-1000 | Tantalum | 35 | 20 | 3.3µ | C13, 63 |
| 21-1003 | Tantalum | 20 | 20 | 15µ | C81 |
| 21-1006 | Tantalum | 35 | 20 | 4.7µ | C29 |
| 21-1029 | Tantalum | 35 | 20 | 1.5µ | C30 |
| 21-1031 | Tantalum | 35 | 20 | 100n | C82 |
| 21-1038 | Tantalum | 6.3 | 20 | 47µ | C2, 8, 10, 15, 17, 21, 23, 25, 26, 33, 56, 58, 68 |
| 21-1039 | Tantalum | 16 | 20 | 22µ | C5, 6, 12, 80 |
| 21-1041 | Tantalum | 35 | 20 | 1µ | C50 |
| 21-1506 | Ceramic | 500 | 10 | 6.8p | C4 |
| 21-1513 | Ceramic | 500 | 10 | 27p | C14 |
| 21-1516 | Ceramic | 500 | 10 | 47p | C1 |
| 21-1532 | Ceramic | 500 | 20 | 1n | C65, 72, 76 |
| 21-1589 | Ceramic | 10 | -20+50 | 220n | C62, 64, 66 |
| 21-1610 | Ceramic | 100 | -20+80 | 10n | C31, 32, 36, 37 38, 40, 42 44, 45, 48, 52, 53, 54, 55, 85, 86, 87, 88 |
| 21-1616 | Ceramic | 12 | -20+80 | 100n | C3, 7, 11, 16, 18, 19, 20, 22, 24, 27, 28, 43, 57, 59, 60, 61, 67, 69, 70 71, 73, 74, 75, 77, 78, 79, 84, 89, 90, 91 |
| 21-1680 | Ceramic | 63 | 0.25p | 10p | C41 |
| 21-1683 | Ceramic | 63 | 2 | 18p | C46 |
| 21-1687 | Ceramic | 63 | 2 | 39p | C51 |
| 21-1728 | Ceramic | 100 | 10 | 220p | C34 |
| 21-1729 | Ceramic | 200 | -20+80 | 10n | C35 |
| | **Diodes** | | | | |
| 22-0007 | Germanium gold bonded (AAZ15) | | | | D37, 38 |
| 22-1029 | Silicon | | | | D1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 16, 19, 20, 21, 23, 24, 25, 26, 27, |
| 22-1033 | Silicon | | | | D17, 18 |
| 22-1058 | Silicon | | | | D11, 12, 13, 14, 15 |
| 22-1602 | Rectifier, 100V, 0.5A (1N4002) | | | | D29, 30, 31, 32, 33, 34, 35, 36 |
| 22-1854 | Voltage regulator 5.1V (BZY88-C5V1) | | | | D28 |

## PARTS LIST FOR FIG. 3 & FIG. 4

### MAIN PCB ASSEMBLY (contd.)

| Part No. | Description | Component Reference |
|---|---|---|
| | **Integrated Circuits** | |
| 22-4040 | 1ØD Bistable (MC1670L) | IC20 |
| 22-4059 | Hex Inverter (7404) | IC14, 24 |
| 22-4111 | Operational Amp (741) | IC32 |
| 22-4202 | Freq. compensated Op Amp (747) | IC22, 29 |
| 22-4204 | UHF Amp (OM335) | IC30 |
| 22-4216 | Transistor Array, npn (CA3083) | IC26, 27 |
| 22-4221 | Differential Video Amp (72733) (Texas only) | IC33 |
| 22-4224 | +24V Regulator | IC34 |
| 22-4520 | 600MHz ÷ 10 (SP8635B) | IC25 |
| 22-4528 | Triple Line Receiver (MC10116P) | IC31 |
| 22-4528 | Presettable Decade, (N82S90A) | IC6 |
| 22-4530 | Quad 2 to 1 Multiplexer (74LS157PC) | IC11 |
| 22-4531 | Quad 2 i/p NAND (74LS00N) | IC7, 28 |
| 22-4532 | Quad 2 i/p NOR (74 LS02N) | IC19 |
| 22-4534 | Dual-D Bistable (74LS74AN) | IC12, 13, 17 |
| 22-4536 | Decade counter | IC2 |
| 22-4546 | Quad 2 i/p NAND (74LS03N) | IC16 |
| 22-4551 | Hex Schmitt inverter (7414N) | IC3 |
| 22-4552 | 4-Bit Adder, Schottky | IC10 |
| 22-4553 | Hex. inverter, open collector (74LS05N) | IC18 |
| 22-4554 | 4-2-3-2 And/or Inverter | IC19 |
| 22-4555 | Dual And/Or Inverter | IC1 |
| 22-4558 | Quad 2 i/p AND | IC21 |
| 22-4559 | Quad 2 i/p NOR | IC15 |
| 22-4601 | CDI Chip-Racal | IC5 |
| 22-4706 | BCD Counter/Decoder CMOS (HEF4017P) | IC13 |
| 22-4718 | Dual 4-bit Latch CMOS | IC4 |
| 22-4719 | Hex Inverter CMOS | IC8 |

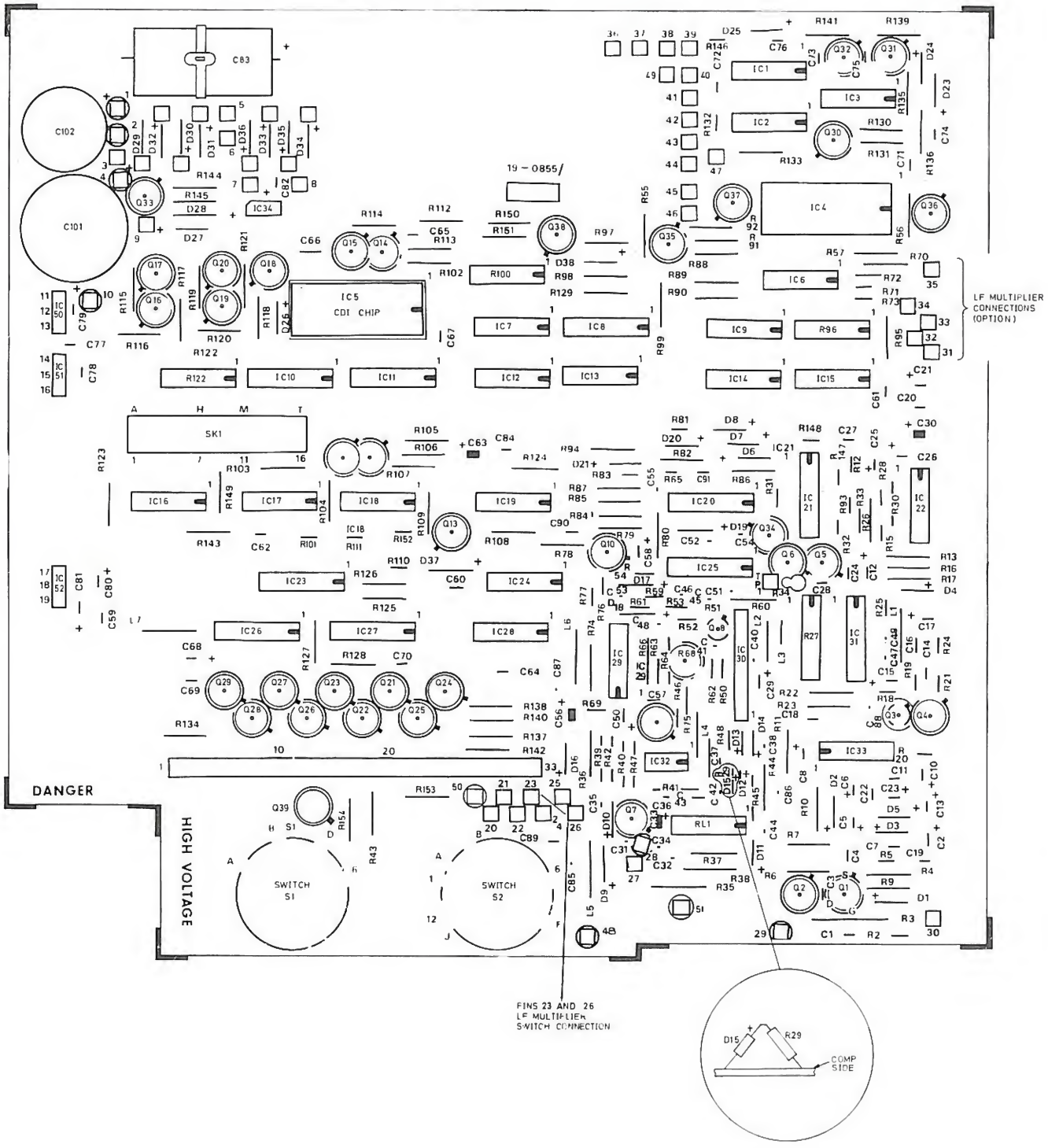
| Part No. | Description | | Component Reference |
|---|---|---|---|
| | **Transistors** | | |
| 22-6009 | Silicon npn (2N4124) | | Q9 |
| 22-6017 | Silicon npn (2N2369) | | Q2, 7, 10, 11, 15, 30, 31, 32, 34, 35, 37, 38 |
| 22-6101 | Silicon FET, N channel (W300A) | | Q1 |
| 22-6110 | Silicon pnp (BFX48) | | Q3, 4, 5, 6, |
| 22-6112 | Silicon npn, high current (ZTX450) | | Q16, 19 |
| 22-6113 | Silicon pnp, high current (ZTX550) | | Q12, 13, 14, 17, 18, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 22, 36 |
| 22-6123 | Silicon npn u.h.f. amp (BFR90) | | Q8 |
| 22-6079 | Silicon npn (ZTX313L) | | Q39 |
| | **Inductors** | | |
| 23-7018 | Choke r.f., sub-min | 47µ | L1 |
| 23-7011 | Choke r.f., sub-min | 3.3µ | L2 |
| 17-3207 | Choke to Racal drg. | | L3 |
| 23-7014 | Choke, r.f. sub-min | 10µ | L4, 5, 7 |
| 23-7016 | Choke, r.f. sub-min | 22µ | L6 |
| | **Switches** | | |
| 17-0106 | Switch to Racal drawing (GATE) | | S1 |
| 17-0107 | Switch to Racal drawing (INPUT) | | S2 |
| | **Miscellaneous** | | |
| 23-7516 | Reed Relay, DIL, 5V | 500 | RL1 |
| 23-5139 | Edge Connector, 16-way | | SK1 |

### DISPLAY ASSEMBLY 19-0858

(Components are prefixed '1' on Fig. 4)

| | Resistors | W | % | Ω | |
|---|---|---|---|---|---|
| 20-5506 | DIL Array (8) | | | 47 | R1, 2 |
| 20-2221 | Carbon Film | ¼ | 5 | 220 | R3 |
| | **Capacitors** | **V** | | **F** | |
| 21-1038 | Tantalum | 6.3 | 20 | 47 | C1, 3 |
| 21-1610 | Ceramic | 100 | -10+80 | 10n | C2 |
| 21-1616 | Ceramic | 12 | -20+80 | 100n | C4 |

| Part No. | Description | Component Reference |
|---|---|---|
| | **Diodes** | |
| 22-1029 | Silicon, general purpose (1N4149) | D1 |
| | **Integrated Circuits** | |
| 22-4128 | 7-segment decoder (SN74247) | IC1 |
| 22-4556 | LP Schottky | IC2 |
| | **Inductors** | |
| 26-1505 | Seven seqment (TIL312) | D1.1-D1.9 |
| 26-5004 | Indicator, l.e.d. red (HP.5082-4484) | LP1-LP6 |

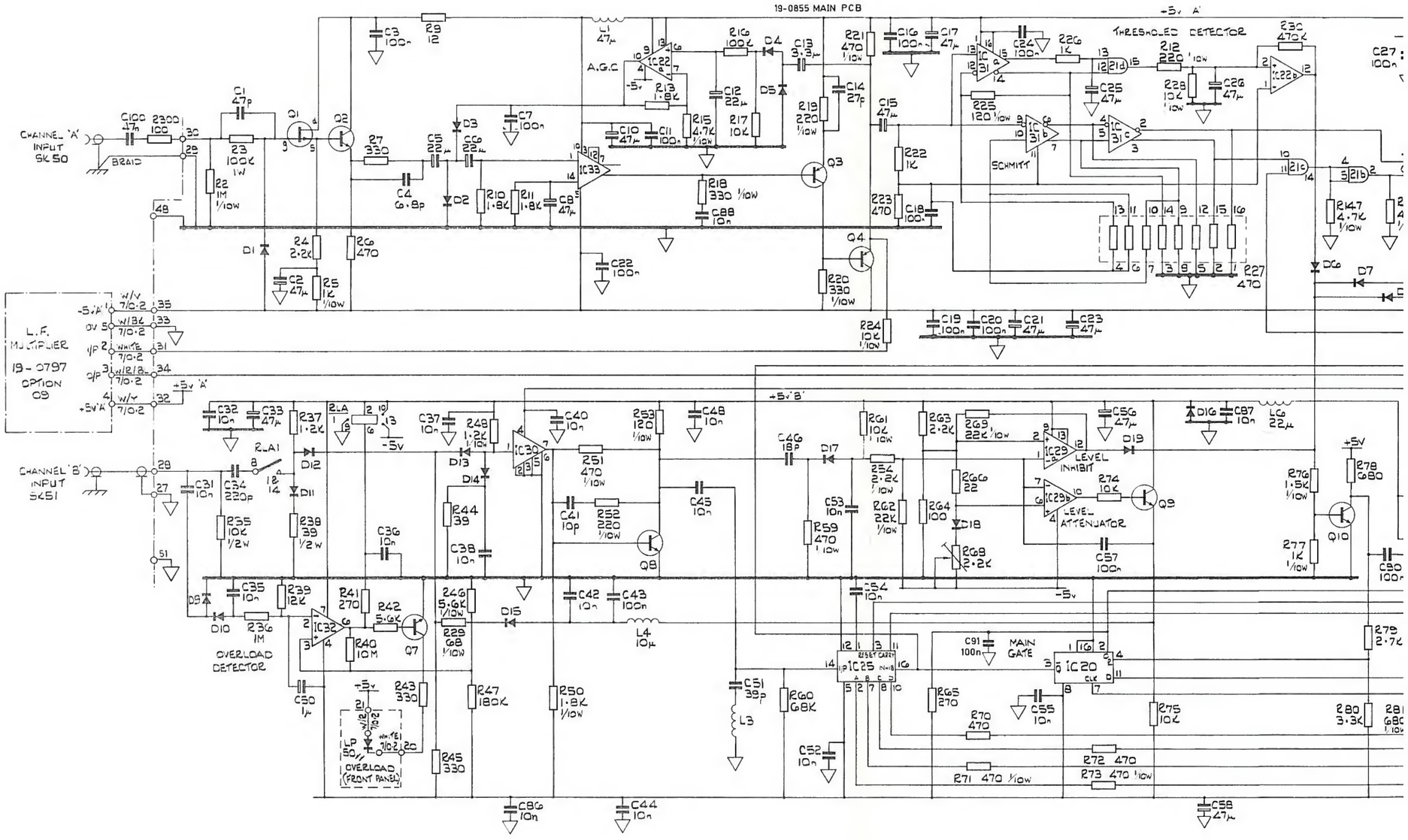



RACAL
WOH8006 | 19-0855
1 2

Component Layout : Main P.C.B Assembly
19-0855

Fig. 2

19-0855 MAIN PCB

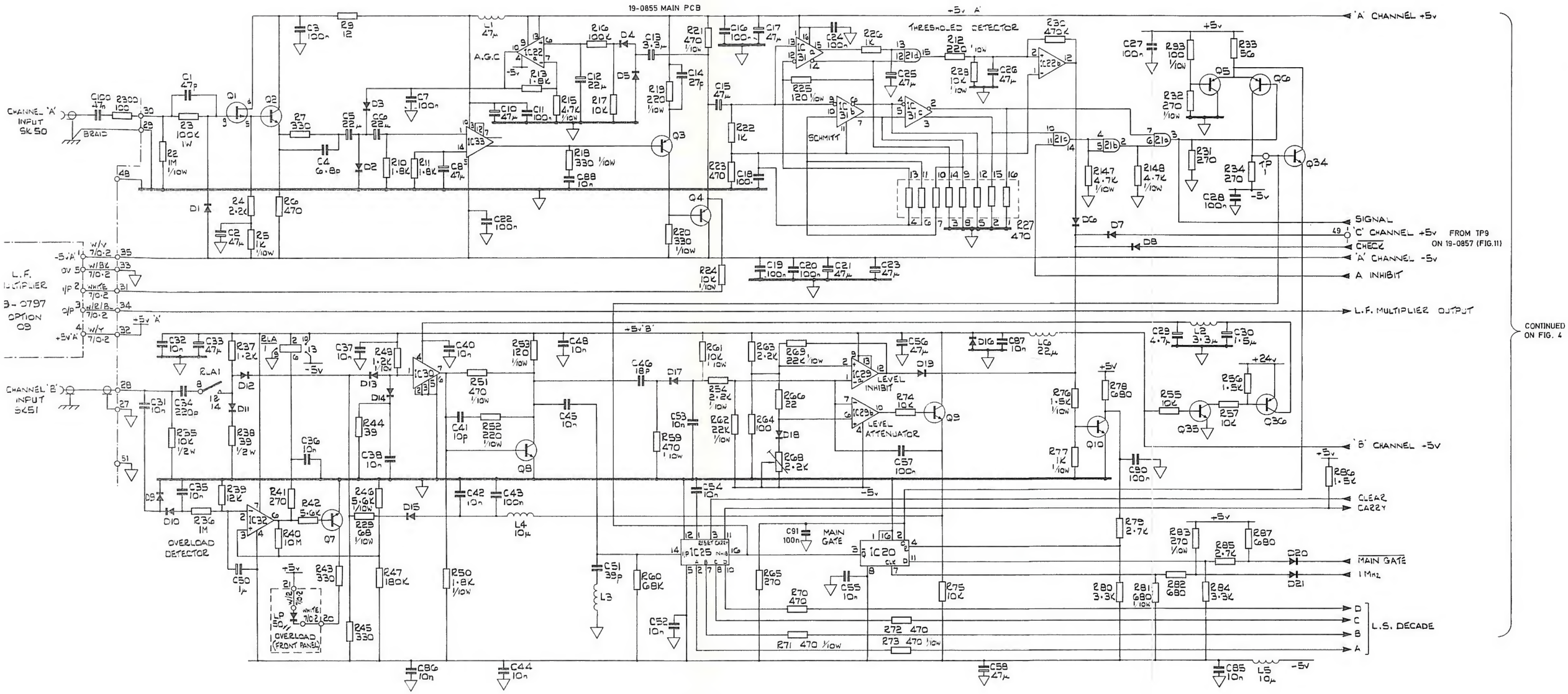



INTEGRATED CIRCUIT SUPPLIES

| REFERENCE | 0V | +5V | +5V 'A' | +5V 'B' | -5V | -5V 'A' | +24V |
|---|---|---|---|---|---|---|---|
| IC20 | 1,16 | | | | 8 | | |
| IC32 | | | | 7 | 4 | | |
| IC22 | | | 9,13 | | | 4 | |
| IC29 | | | | 9,13 | 4 | | |
| IC30 | 2,3,5 | | | | | | 4 |
| IC33 | | | 10 | | | 5 | |
| IC25 | 12 | | | | 5 | | |
| IC31 | 8 | | 1,16 | | | | |
| IC21 | 8 | 1,16 | | | | | |

RACAL

| WOH 8006 | 9921 SHT 2 |
|---|---|
| 1 | 2 |




INTEGRATED CIRCUIT SUPPLIES

| REFERENCE | 0V | +5V | +5V'A' | +5V'B' | -5V | -5V'A' | +24V |
|---|---|---|---|---|---|---|---|
| IC20 | 1,16 | | | | 8 | | |
| IC32 | | | | 7 | 4 | | |
| IC22 | | | 9,13 | | | 4 | |
| IC29 | | | | 9,13 | 4 | | |
| IC30 | 2,3,5 | | | | | | 4 |
| IC33 | | | 10 | | | 5 | |
| IC25 | 12 | | | | 5 | | |
| IC31 | 8 | | 1,16 | | | | |
| IC21 | 8 | 1,16 | | | | | |

AGAL
DH 8006 9921 SHT 2
2

Overall Circuit :
9918 & 9921 (Part 1)

Fig. 3

PART OF 19-0855 MAIN P.C.B.

DISPLAY DRIVERS

OFF CHIP DECADE STORES

SPARE

H.S. DECADE

OVERFLOW DETECTOR

DISPLAY TIME GENERATOR

'C' CHECK AND 'C' CHANNEL GATING

'C' SIGNAL

CONTROL RESET AND UPDATE

INT/EXT. SELECT GATE

EXT. STD. I/P AND DETECTOR

9442 OSCILLATOR

SIDE PANEL

REMOTE

GATE TIME SWITCH

FREQUENCY I/P LATCH/UNLATCH AUTO

OFF CHIP GATE CONTROL

EXT. STD INPUT

MAIN GATE

IC5 CDI CHIP

REMOTE AND BCD SOCKET FOR OPTION 02 19-0859

REMOTE COMMAND

BCD DATA

POWER ON/OFF

+5V LOGIC SUPPLY

CHECK AND 'C' CHANNEL GATING

'C' SIGNAL

CONTROL RESET AND UPDATE

DISPLAY TIME GENERATOR

FREQUENCY I/P LATCH/UNLATCH AUTO
1MHz/500KHz O/P
MAIN GATE
+2V
V REF
STOP 10MHz
O.C.G.C.
OFF CHIP GATE CONTROL
HOLD RESET
10KHz/5KHz
EXT. STD. INPUT
IC5
CDI CHIP

MAIN GATE
10 KHz/5 KHz
HOLD/RESET
0V
REMOTE AND BCD SOCKET FOR OPTION 02 19-0859
SK1
REMOTE COMMAND
LF REMOTE
REMOTE SWITCH ON
+5V OSC.
"BCD DATA"
"D.P. DATA"
STATE COUNTER HOLD
O/F

GATE TIME SWITCH
10mS
100mS
1S
10S
S1
OPTION 09
S51
LF
HF
FRONT PANEL
'C' SELECT
'B' SELECT
CHECK

19-0858 DISPLAY ASSY.

INT/EXT. SELECT GATE
500KHZ(C)
1MHZ (A&B)
9442 OSCILLATOR
W/G 7/0-2 LINK*
EXT. STD. I/P AND DETECTOR
EXT. STD. I/F
1MHz STD. O/P

SIDE PANEL
IC50
IC51
IC52
IC34
+5V LOGIC SUPPLY
-5.2V
+24V

S2a
S2b
CHANNEL AND REMOTE SELECT

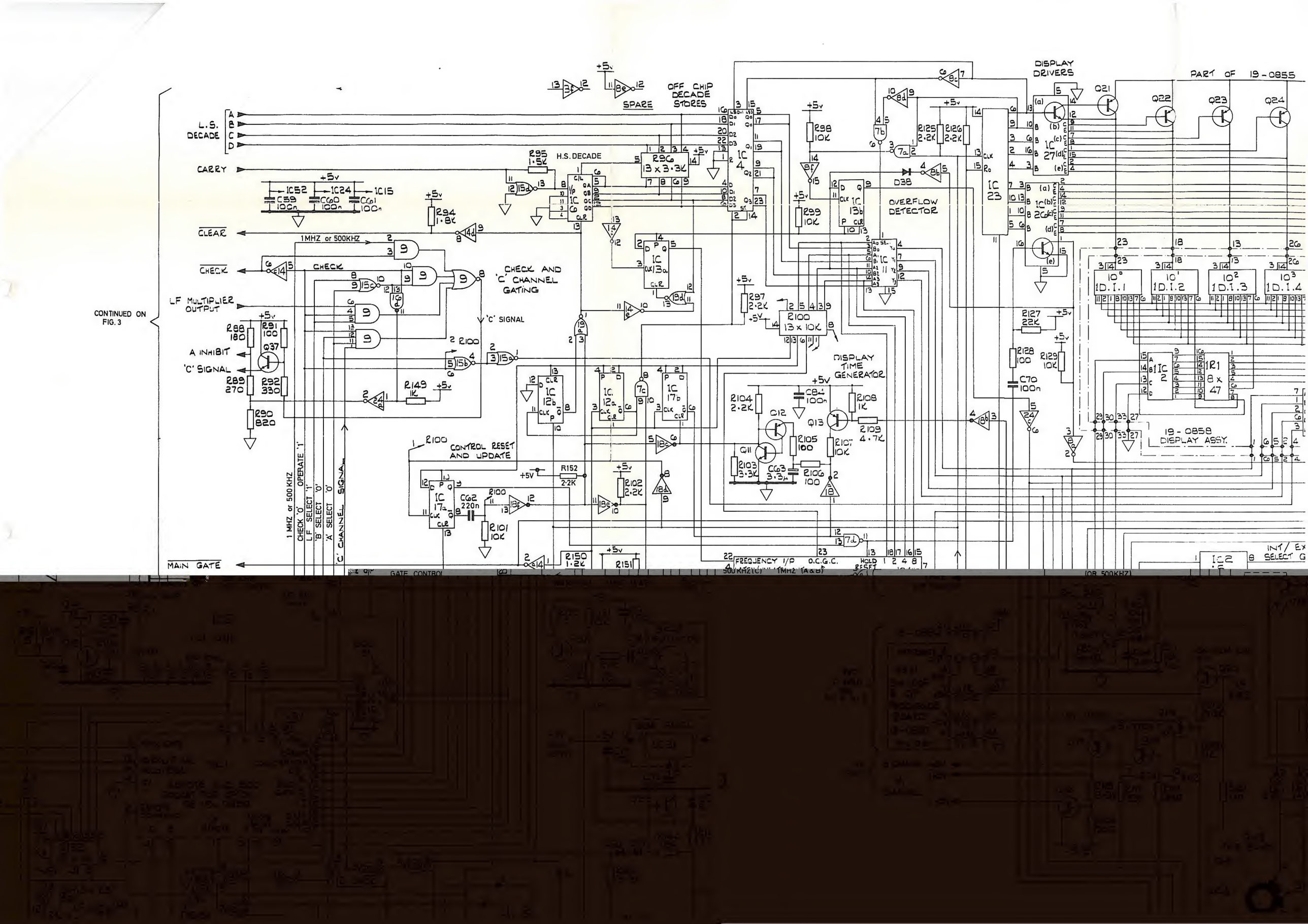
REMOTE +5V
O/F STD BY
1MHz
1Hz
GATE
EXT. STD.

TS0
120V
105V
115V
125V
POWER ON/OFF
S54
MAINS FILTER AND CONNECTOR

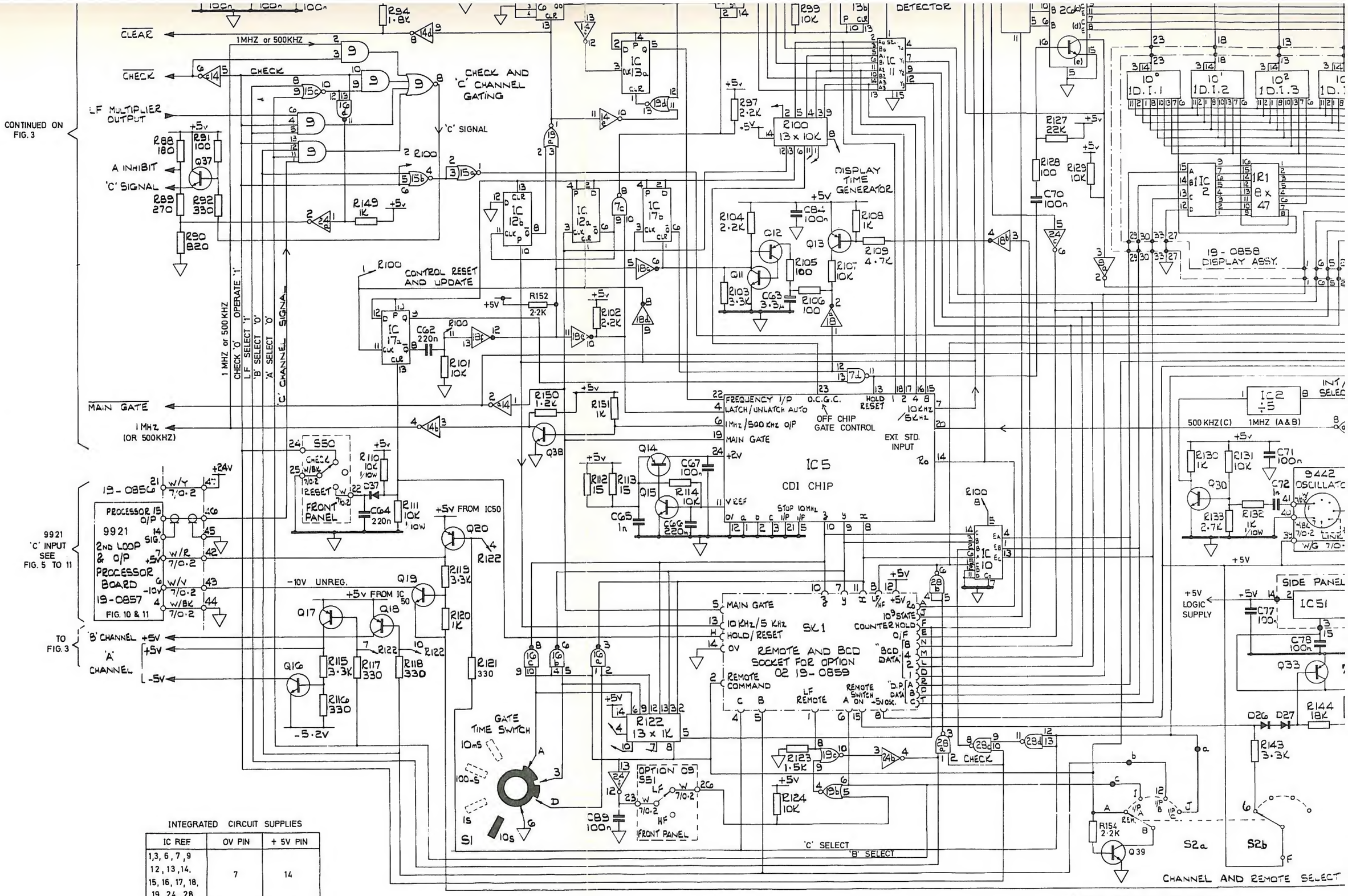
* NOTE: LINK FITTED ON OSCILLATOR BASE WITH 9421 ONLY.

Overall Circuit 9918 & 9921 (Part 2)

Fig. 4



L.S. DECADE
CARRY
CLEAR
CHECK
LF MULTIPLIER OUTPUT
A INHIBIT
'C' SIGNAL
MAIN GATE
CONTINUED ON FIG. 3
1MHZ or 500KHZ
CHECK
CHECK AND 'C' CHANNEL GATING
'C' SIGNAL
H.S. DECADE
SPARE
OFF CHIP DECADE STORES
OVERFLOW DETECTOR
DISPLAY DRIVERS
PART OF 19-0855
DISPLAY TIME GENERATOR
CONTROL RESET AND UPDATE
1 MHZ or 500 KHZ
CHECK '0' OPERATE '1'
LF SELECT '1'
'B' SELECT '0'
'A' SELECT '0'
'C' CHANNEL SIGNAL
GATE CONTROL
FREQUENCY I/P
O.C.G.C.
HOLD
RESET
19-0858 DISPLAY ASSY.
INT/EX SELECT




INTEGRATED CIRCUIT SUPPLIES

| IC REF | OV PIN | + 5V PIN |
|---|---|---|
| 1,3, 6, 7, 9 12, 13, 14, 15, 16, 17, 18, 19, 24, 28 | 7 | 14 |
| 8, 11, 23 | 8 | 16 |
| | | |
| 4 | 12 | 24 |
| 10 | 11, 12, 18 | 16 |
| 26, 27 | 5 | – |

* NOTE: LINK FITTED ON OSCILLATOR BASE WITH 9421 ONLY.

WOH8006 9921 SHEET 3
1 2

# Overall Circuit 9918 & 9

## PARTS LIST FOR FIG. 6 & FIG. 7

## TOP LOOP AND SAMPLER ASSEMBLY 19-0856

**NOTE**

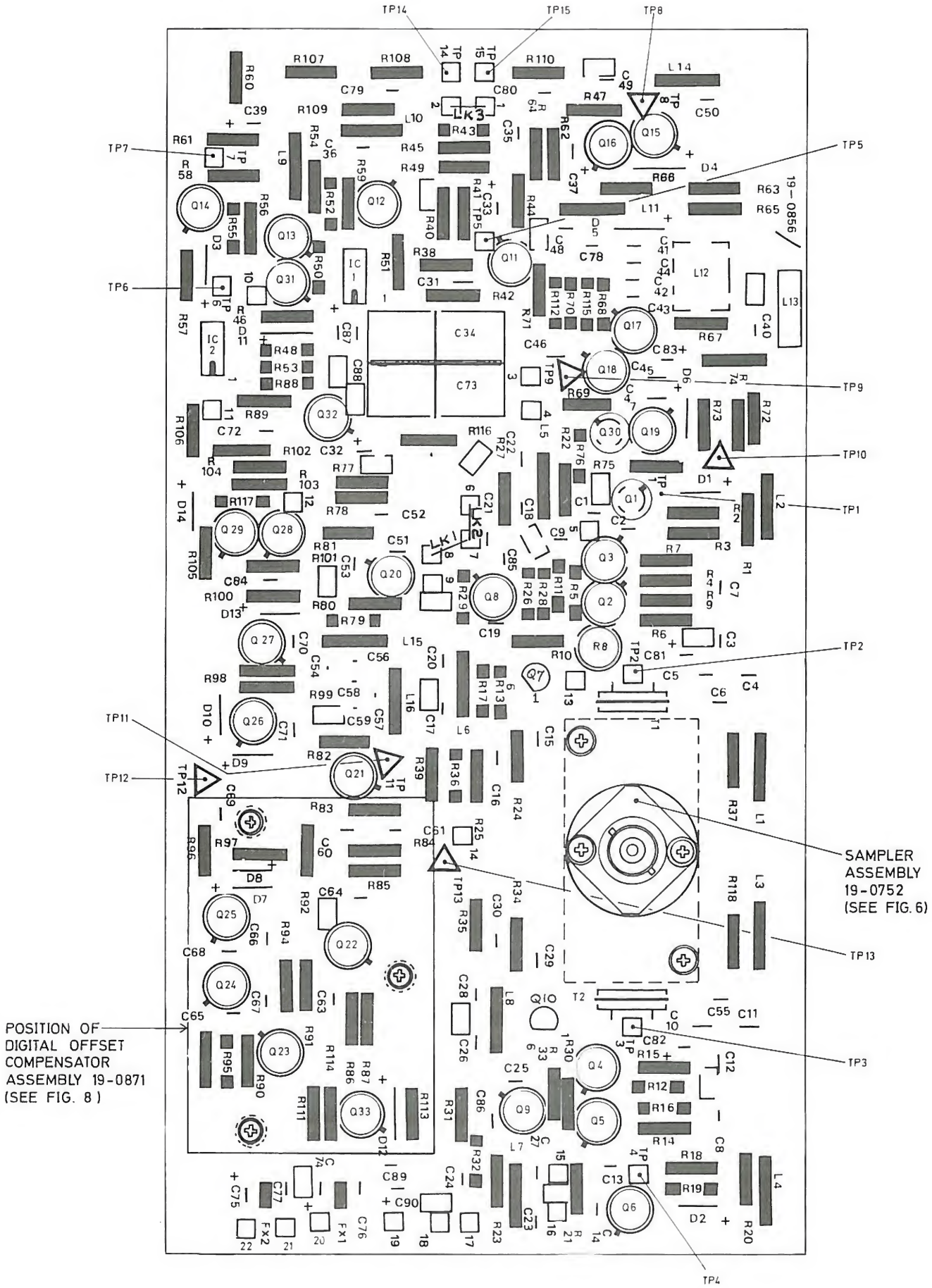
**SAMPLER SUB-ASSEMBLY 19-0752**

This Sub-Assembly should be returned to Racal Instruments Ltd, or Company agents, for repair or replacement. No. Parts List information is provided in this handbook.

19-0856

| Part No. | Description | Rat | Tol % | Value | Component Reference |
|---|---|---|---|---|---|
| | **Resistors** | W | | Ω | |
| 20-2100 | Carbon Film | ¼ | 5 | 10 | R43,53 |
| 20-2101 | Carbon Film | ¼ | 5 | 100 | R27,32,47,115 |
| 20-2102 | Carbon Film | ¼ | 5 | 1k | R2,19,40,41 46,52,54,57,70, 71,102 |
| 20-2103 | Carbon Film | ¼ | 5 | 10k | R5,22,23,36, 39,42,51,58, 59,88,89,94, 95,98,100,103 |
| 20-2122 | Carbon Film | ¼ | 5 | 1.2k | R79,82 |
| 20-2123 | Carbon Film | ¼ | 5 | 12k | R105 |
| 20-2151 | Carbon Film | ¼ | 5 | 150 | R63 |
| 20-2152 | Carbon Film | ¼ | 5 | 1.5k | R80,97 |
| 20-2154 | Carbon Film | ¼ | 5 | 150k | R24,25,34,35 |
| 20-2181 | Carbon Film | ¼ | 5 | 180 | R75 |
| 20-2182 | Carbon Film | ¼ | 5 | 1.8k | R11,26 |
| 20-2183 | Carbon Film | ¼ | 5 | 18k | R68,101,104 |
| 20-2221 | Carbon Film | ¼ | 5 | 220 | R50,62,76,111 |
| 20-2222 | Carbon Film | ¼ | 5 | 2.2k | R37,61,67,92 113,114,118 |
| 20-2223 | Carbon Film | ¼ | 5 | 22k | R65 |
| 20-2272 | Carbon Film | ¼ | 5 | 2.7k | R73,90,93 |
| 20-2273 | Carbon Film | ¼ | 5 | 27k | R72 |
| 20-2331 | Carbon Film | ¼ | 5 | 330 | R14 |
| 20-2332 | Carbon Film | ¼ | 5 | 3.3k | R29,31,38, 60,85 |
| 20-2333 | Carbon Film | ¼ | 5 | 33k | R1,20 |
| 20-2391 | Carbon Film | ¼ | 5 | 390 | R74,112 |
| 20-2393 | Carbon Film | ¼ | 5 | 39k | R66 |
| 20-2471 | Carbon Film | ¼ | 5 | 470k | R3,18,33,45, 48,69 |
| 20-2472 | Carbon Film | ¼ | 5 | 4.7k | R83,91 |
| 20-2473 | Carbon Film | ¼ | 5 | 47k | R10,17 |
| 20-2560 | Carbon Film | ¼ | 5 | 56 | R6,9,12, 15, 21,28,30,44, 49,64 |
| 20-2561 | Carbon Film | ¼ | 5 | 560 | R4,16 |
| 20-2562 | Carbon Film | ¼ | 5 | 5.6k | R96 |
| 20-2563 | Carbon Film | ¼ | 5 | 56k | R56, 106 |
| 20-2680 | Carbon Film | ¼ | 5 | 68 | R13 |
| 20-2681 | Carbon Film | ¼ | 5 | 680 | R7, 86, 87 |
| 20-2682 | Carbon Film | ¼ | 5 | 6.8k | R99 |
| 20-2683 | Carbon Film | ¼ | 5 | 68k | R55 |
| 20-2684 | Carbon Film | ¼ | 5 | 680k | R116 |
| 20-2821 | Carbon Film | ¼ | 5 | 820 | R81 |
| 20-2822 | Carbon Film | ¼ | 5 | 8.2k | R77,78,84,117 |
| 20-4007 | Metal Oxide | ¼ | 2 | 2.2k | R108,109 |
| 20-4061 | Metal Oxide | ¼ | 2 | 6.8k | R110 |
| 20-4071 | Metal Oxide | ¼ | 2 | 3.3k | R107 |
| 20-7025 | Variable, cermet | | | 200 | R8 |
| | **Inductors** | | | | |
| 23-7081 | Choke | | | 100uH | L1,2,3,4,5,6,7, 8,9,10,13,14, |
| 23-7072 | Choke | | | 10uH | L11 |
| 23-7073 | Choke | | | 12uH | L16 |
| 23-7074 | Choke | | | 15uH | L15 |
| 17-3201 | Coil Assembly to Racal Drg | | | | L12 |
| 17-4065 | Transformer, pulse. | | | | T1,2 |
| 23-8000 | Ferrite Bead | | | | FX1,2 |

| Part No. | Description | Rat | Tol % | Value | Component Reference |
|---|---|---|---|---|---|
| | **Capacitors** | V | | F | |
| 21-1002 | Tantalum | 20 | 20 | 10µ | C32,33,39,74,75, 81,82,83,87, , |
| 21-1038 | Tantalum | 6.3 | 20 | 47µ | C37 |
| 21-1040 | Tantalum | 35 | 20 | 6.8µ | C90 |
| 21-1520 | Ceramic | 500 | 10 | 100p | C43,51 |
| 21-1524 | Ceramic | 500 | 10 | 220p | C63,69 |
| 21-1530 | Ceramic | 500 | 10 | 680p | C64 |
| 21-1545 | Ceramic | 25 | -20+80 | 10n | C6,9,35,55,89 |
| 21-1547 | Ceramic | 18 | -20+50 | 33n | C70 |
| 21-1616 | Ceramic | 12 | -20+80 | 100n | C1,2,3,4,5,7,8, 10,11,12,13,14,15, 16,17,18,19,20,21, 22,23,24,25,26,27, 28,29,30,31,36,40, 41,44,45,46,47,48, 49,50,52,53,60,61, 65,66,67,68,71,72, 76,77,78,79,80,84, 85,86,88 |
| 21-1673 | Ceramic | 63 | 0.25p | 2.7p | C56 |
| 21-1678 | Ceramic | 63 | 0.25p | 6.8p | C57 |
| 21-1683 | Ceramic | 63 | 2 | 18p | C59 |
| 21-1684 | Ceramic | 63 | 2 | 22p | C54 |
| 21-1635 | Ceramic | 63 | 2 | 27p | C58 |
| 21-1720 or 21-2632 | Ceramic or Silver Mica | 100 | 5 | 470p | C42 |
| 21-4557 or 21-5509 | Polyester or Polycarbonate | 100 | 20 | | C34,73 |
| | **Diodes** | | | | |
| 22-1029 | Silicon, general purpose (IN4149) | | | | D1,2,3,6,7,8,9,10, 13,14 |
| 22-1032 | Variable Capacitors (MV.1650) | | | | D5 |
| 22-1801 | Voltage reg. 2.7V (BZX-83C-2V7) | | | | D11 |
| 22-1808 | Voltage reg. 5.1V (BZY-88C-5V1) | | | | D4 |
| 22-1817 | Voltage reg. 12V (BZY-88C-12) | | | | D12 |
| | **Integrated Circuits** | | | | |
| 22-4111 | Operational amp. (741) | | | | IC2 |
| 22-4201 | Operational amp. (LM307N) | | | | IC1 |
| | **Transistors** | | | | |
| 22-6010 | Silicon, pnp. (2N4126) | | | | Q14 |
| 22-6041 | Silicon, npn. (BC.109) | | | | Q12,27,29 |
| 22-6079 or 22-6017 | Silicon, npn. (ZTX.313L) or Silicon, npn. (2N2369) | | | | Q1,2,3,4,5,6,8,9, 11,13,17,18,19,20, 21,22,23,24,25,26, 28,30,32,33 |
| 22-6110 | Silicon, pnp. (BFX.48) | | | | Q31 |
| 22-6113 | Silicon, pnp, high circuit (ZTX.550) | | | | Q15,16 |
| 22-6119 | Dual FET (E401) | | | | Q7,10 |

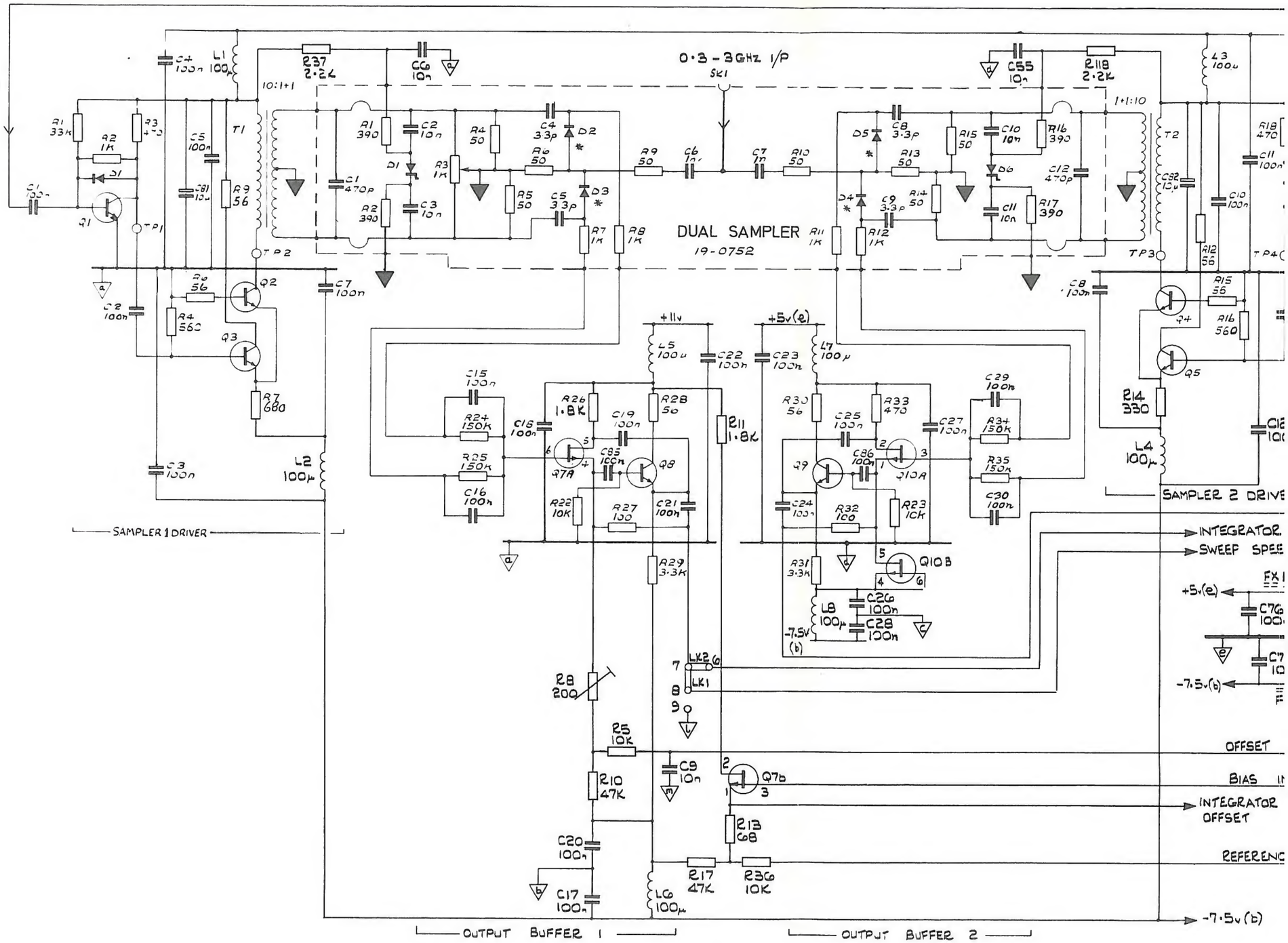



RACAL

| WOH 8006 | 19-0856 SHT 1 |
|---|---|
| 1 | |

# Component Layout : Top Loop and Sampler Assembly 19-0856

Fig. 5




NOTES : 1. ▼ SYMBOL DENOTES GROUND PLANE EARTH
2. * MATCHED DIODE QUAD

RACAL

| WOH8006 | 19 0856 Sht. 2 |
|---|---|
| 1 | |

DRIVE 1 FROM OSCILLATOR (FIG. 7)

+5V(e)

0·3 - 3GHz I/P SK1

10:1:1

1:1:10

DUAL SAMPLER 19-0752

SAMPLER 1 DRIVER

SAMPLER 2 DRIVER

OUTPUT BUFFER 1

OUTPUT BUFFER 2

DRIVE TO SAMPLER 2

1 OSCILLATOR OUTPUT
2 0V

PART OF 19-0857 2ND LOOP AND OUTPUT PROCESSOR ASSY. (FIG. 10 & FIG. 11)

SAMPLER 2 OUTPUT 17 / 18

12 PROCESSOR INPUT
13 0V

INTEGRATOR INPUT
SWEEP SPEED UP INPUT
} FIG. 7

W/R 7/0.2 — 5 +5V(d)
W/BK 7/0.2 — 4 0V
W/S 7/0.2 — 3 -7.5V(a)

+5V(e) — FX1 — 20 — W/R 7/0.2 — 8 +5V(d)
C76 100n, C74 10µ
21 — W/BK 7/0.2 — 9 0V
C77 100n, C75 10µ
-7.5V(b) — FX2 — 22 — W/S 7/0.2 — 7 -7.5V(a)

PART OF 19-0871 DIGITAL OFFSET COMR ASSY. (FIG. 8)

OFFSET OUTPUT — 5 W/R/Y 7/0.2 — 3 OFFSET INPUT
BIAS INPUT — 13 W/R/BL 7/0.2 — 1 BIAS OUTPUT
INTEGRATOR OFFSET
REFERENCE OUTPUT — 14 W 7/0.2 — 2 REFERENCE INPUT

-7·5V(b)

NOTES : 1. ▽ SYMBOL DENOTES GROUND PLANE EARTH
2. * MATCHED DIODE QUAD

ACAL H8006 | 19 0856 Sht. 2

Circuit : Top Loop & Sampler Assembly 19-0856 (Part 1)
Fig. 6

PART OF 19-0855 MOTHER BOARD ASSY.

+24v 47 W/Y 7/0.2 19 +24v

SWEEP RESET 4 W 7/0.2 11

PART OF 19-0871 DIGITAL OFFSET COMP. ASSY. (FIG. 8)

INTEGRATOR OFFSET

INTEGRATOR INPUT

RAMP UP 6 W/R/Y 7/0.2 10

SWEEP SPEED - UP 5 W/R/B 7/0.2 12

SWEEP SPEED - UP INPUT (FIG. 6)

LOOP INTEGRATOR AND SWEEP

REGULATOR

19 - 21 MHz OSCILLATOR

BUFFER

SWEEP SPEED - UP

RACAL

| WOH 8006 | 19-0856 SHT. 3 |
|---|---|
| 1 | 2 |

Top Loop and S
19-0856

PART OF 19-0855 MOTHER BOARD ASSY.

PART OF 19-0871 DIGITAL OFFSET COMP. ASSY. FIG. 8)

+24v

47 W/Y 7/0.2 19

4 W 7/0.2 11

SWEEP RESET

6 W/R/Y 7/0.2 10

RAMP UP

5 W/R/B 7/0.2 12

SWEEP SPEED - UP

INTEGRATOR OFFSET

INTEGRATOR INPUT

+5v(e)

PART OF 19-0857 2ND LOOP AND OUTPUT PROCESSOR

OSC. OUTPUT

DIVIDER INPUT (FIG. 10)

DRIVE I TO SAMPLER (FIG. 6)

+11v

TP13

TP14

TP15

TP8

TP9

TP10

TP11

TP12

TP7

TP5

LK3

IC1

IC2

Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q30 Q31 Q32 Q33

D3 D4 5·1v D5 D6 D9 D10 D11 2·7v D12 12v D13 D14

L8 100µ L9 100µ L10 100µ L11 10µ L12 1µ L13 100µ L14 100µ L15 13µ L16 12µ

R239 10K R242 10K R243 3·3K R244 56 R245 470 R246 1K R247 100 R249 470 R250 220 R251 10K R252 1K R254 1K R255 68K R256 56K R257 10K R258 10K R259 10K R260 3·3K R261 2·2K R262 3·3K R263 150 R264 56 R265 22K R266 39K R267 2·2K R268 18K R269 470 R270 1K R271 1K R272 27K R273 2·7K R274 390 R275 150 R276 220 R277 8·2K R278 8·2K R279 1·5K R280 1·5K R281 820 R282 1·2K R283 4·7K R284 8·2K R285 680 R286 2·2K R287 10K R288 10K R289 10K R290 2·7K R291 2·7K R292 2·2K R293 2·7K R294 10K R295 10K R296 5·6K R297 1·5K R298 10K R299 6·8K R100 10K R101 18K R102 1K R103 10K R104 18K R105 12K R106 56K R107 3·3K 2% R108 2·2K 2% R109 2·2K 2% R110 6·8K 2% R111 220 R112 390 R113 2·2K R114 2·2K R116 680K

C31 100n C32 10µ C33 10µ C34 2·2µ C35 10µ C36 100n C37 47µ C38 10µ C39 10µ C40 100n C41 100n C42 470p ±5% C43 100n C44 100n C45 100n C46 100n C47 100n C48 100n C49 100n C50 100n C51 100n C52 100n C53 100n C54 22p ±2% C55 6·8p ±2% C56 2·7p ±0·25p C57 6·8p ±0·25p C58 2·7p ±0·25p C59 18p ±2% C60 100n C61 100n C62 220p C63 220p C64 680p C65 100n C66 100n C67 100n C68 100n C69 100n C70 33n C71 100n C72 100n C73 2·2µ C74 100n C75 100n C76 100n C77 100n C78 100n C79 100n C80 100n C81 100n C82 100n C83 100n C84 100n C85 100n C86 100n C87 10µ C88 100n C89 10n C90 6·8µ

REGULATOR

LOOP INTEGRATOR AND SWEEP

19 - 21 MHz OSCILLATOR

BUFFER

SWEEP SPEED - UP INPUT (FIG. 6)

To -7·5v (b)

To -7·5v (b)

ACAL
DH 8006 | 19-0856 SHT. 3
2

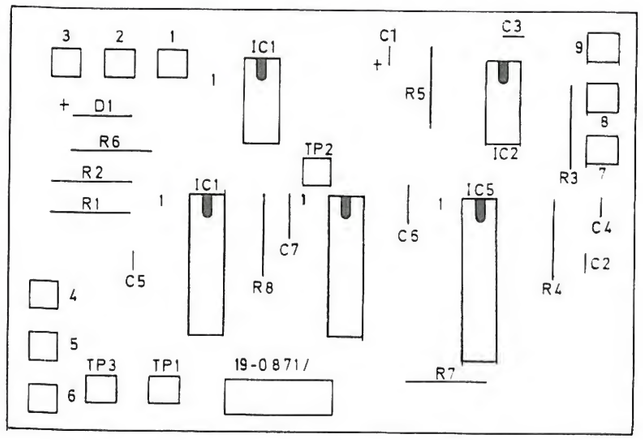
# Top Loop and Sampler Assembly 19-0856 (Part 2)

Fig. 7

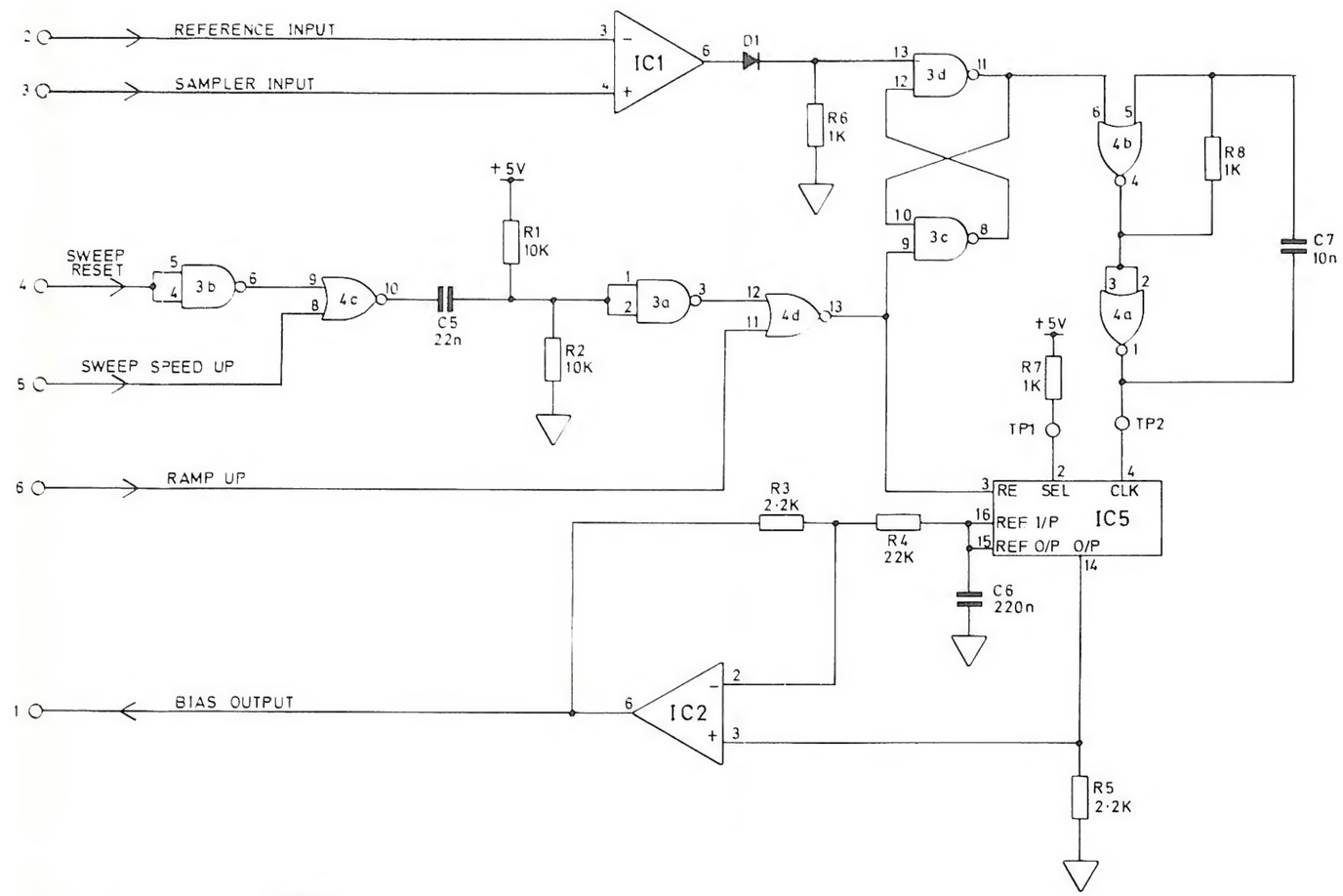
# PARTS LIST FOR FIG. 8

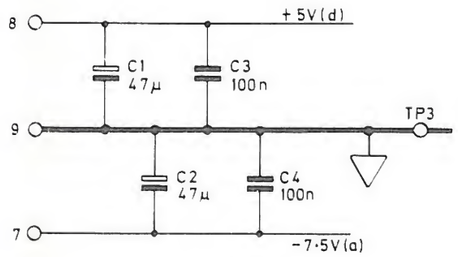
## DIGITAL OFFSET COMPENSATOR ASSEMBLY 19-0871

| Part No. | Description | Rating | Tol. % | Value | Circuit Reference |
|---|---|---|---|---|---|
| | Resistors | W | | | |
| 20-2103 | Carbon Film | ¼ | 5 | 10k | R1,2 |
| 20-2222 | Carbon Film | ¼ | 5 | 2.2k | R3,5 |
| 20-2223 | Carbon Film | ¼ | 5 | 22k | R4 |
| 20-2102 | Carbon Film | ¼ | 5 | 1k | R6,7,8. |
| | Capacitors | V | | F | |
| 21-1038 | Tantalum | 6.3 | 20 | 47u | C1 |
| 21-1045 | Tantalum | 16 | 20 | 47u | C2 |
| 21-1616 | Ceramic | 12 | -20+80 | 100n | C3,4 |
| 21-1546 | Ceramic | 25 | -20+80 | 22n | C5 |
| 21-1589 | Ceramic | 10 | -20+80 | 220n | C6 |
| 21-1544 | Ceramic | 500 | 25 | 10n | C7 |
| | Diodes | | | | |
| 22-1029 | Silicon, general purpose (1N4149) | | | | D1 |
| | Integrated Circuits | | | | |
| 22-4225 | Op. Amp., high speed | | | | IC1 |
| 22-4111 | Op. Amp. | | (741) | | IC2 |
| 22-4531 | Quad 2 i/p NAND | | (74 LS00) | | IC3 |
| 22-4532 | Quad 2 i/p NOR | | (74 LS02) | | IC4 |
| 22-4226 | 8-bit D. to A. converter | | | | IC5 |




COMPONENT LAYOUT




INTEGRATED CIRCUITS SUPPLIES

| IC REF | +5V (d) PIN | -7·5V (a) PIN | 0V PIN |
|---|---|---|---|
| IC1 | 1 | 7 | |
| IC2 | 7 | 4 | |
| IC3 | 14 | | 7 |
| IC4 | 14 | | 7 |
| IC5 | 8 | | 1 |

RACAL

| WOH8006 | 19-0871 |
|---|---|
| 1 | |

Circuit and Component Layout :
Digital Offset Compensator
Assembly 19-0871

Fig.8

## PARTS LIST FOR FIG.10 & FIG.11

### 2ND LOOP AND OUTPUT PROCESSOR ASSEMBLY 19-0857

| Part No. | Description | Rat | Tol | Value | Component Reference |
|---|---|---|---|---|---|
| | **Resistors** | W | % | | |
| 20-2101 | Carbon Film | ¼ | 5 | 100 | R61,57,79 |
| 20-2102 | Carbon Film | ¼ | 5 | 1k | R1,16,18,29, 53,64 |
| 20-2103 | Carbon Film | ¼ | 5 | 10k | R58 |
| 20-2122 | Carbon Film | ¼ | 5 | 1.2k | R27,34,67 |
| 20-2151 | Carbon Film | ¼ | 5 | 150 | R8,78 |
| 20-2154 | Carbon Film | ¼ | 5 | 150k | R63 |
| 20-2181 | Carbon Film | ¼ | 5 | 180 | R21,71,75 |
| 20-2183 | Carbon Film | ¼ | 5 | 18k | R14 |
| 20-2221 | Carbon Film | ¼ | 5 | 220 | R28,35,76 |
| 20-2222 | Carbon Film | ¼ | 5 | 2.2k | R13,26,45 |
| 20-2223 | Carbon Film | ¼ | 5 | 22k | R10,77 |
| 20-2224 | Carbon Film | ¼ | 5 | 220k | R62 |
| 20-2272 | Carbon Film | ¼ | 5 | 2.7k | R56,60,68,73 |
| 20-2331 | Carbon Film | ¼ | 5 | 330 | R7 |
| 20-2332 | Carbon Film | ¼ | 5 | 3.3k | R37,39,52,69 |
| 20-2391 | Carbon Film | ¼ | 5 | 390 | R19,46,47 |
| 20-2392 | Carbon Film | ¼ | 5 | 3.9k | R44,48 |
| 20-2393 | Carbon Film | ¼ | 5 | 39k | R11 |
| 20-2471 | Carbon Film | ¼ | 5 | 470 | R4,5,15,20, 80,81 |
| 20-2472 | Carbon Film | ¼ | 5 | 4.7k | R3,6,9,22, 43,65 |
| 20-2560 | Carbon Film | ¼ | 5 | 56 | R12,24 |
| 20-2561 | Carbon Film | ¼ | 5 | 560 | R23,33,36,54,66 |
| 20-2562 | Carbon Film | ¼ | 5 | 5.6k | R31,32,49 |
| 20-2681 | Carbon Film | ¼ | 5 | 680 | R40,41,72 |
| 20-2682 | Carbon Film | ¼ | 5 | 6.8k | R2,17,74 |
| 20-2822 | Carbon Film | ¼ | 5 | 8.2k | R38,50,51 |
| 20-7027 | Variable, miniature | | | 20k | R59 |
| 20-7035 | Variable, cermet | | | 4.7k | R25 |

| Part No. | Description | Rat | Tol | Value | Component Reference |
|---|---|---|---|---|---|
| | **Capacitors** | V | % | F | |
| 21-1002 | Tantalum | 20 | 10 | 10µ | C7,9,13,25 64,66,68,69 70,71,72,73 |
| 21-1000 | Tantalum | 35 | 20 | 3.3 | C47,74 |
| 21-1038 | Tantalum | 6.3 | 20 | 47p | C45 |
| 21-1520 | Ceramic | 500 | 10 | 100p | C17,50,76 |
| 21-1522 | Ceramic | 500 | 10 | 150p | C32 |
| 21-1525 | Ceramic | 500 | 10 | 270p | C60 |
| 21-1526 | Ceramic | 500 | 10 | 330p | C46 |
| 21-1530 | Ceramic | 500 | 10 | 680p | C44 |
| 21-1532 | Ceramic | 500 | 20 | 1n | C26,54,55 |
| 21-1551 | Ceramic | 25 | -20+80 | 100n | C30 |
| 21-1616 | Ceramic | 12 | -20+80 | 100n | C1,2,3,4,5,6,8,11, 12,14,15,18,19,20, 21,22,23,24,27,28, 29,31,39,33,41,42, 43,48,49,51,52,53, 56,57,58,59,61,62, 63,65,67,75,77,78 |
| 21-1677 | Ceramic | 63 | 0.25p | 5.6p | C36 |
| 21-1679 | Ceramic | 63 | 0.25p | 8.2p | C34 |
| 21-1682 | Ceramic | 63 | 2 | 15p | C38 |
| 21-1690 | Ceramic | 63 | 2 | 68p | C35,40 |
| 21-1692 | Ceramic | 63 | 2 | 100p | C37 |
| 21-1720 or 21-2632 | Ceramic or Silver Mica | 100 | 20 | 470p | C16 |
| 21-4508 or 21-4550 or 21-5503 | Polyester or Polyester or Polycarbonate | 100 | 20 | 220n | C10 |

| Part No. | Description | Value | Component Reference |
|---|---|---|---|
| | **Inductors** | | |
| 23-7081 | Choke | 100uH | L1,2,3,4,5, 6,12,13,14, 15,16 |
| 17-3201 | Coil assembly to Racal drg. | | L7 |
| 23-7034 | Choke | 3.3uH | L9 |
| 23-7072 | Choke | 10uH | L8,11,17 |
| 23-7073 | Choke | 12uH | L10 |

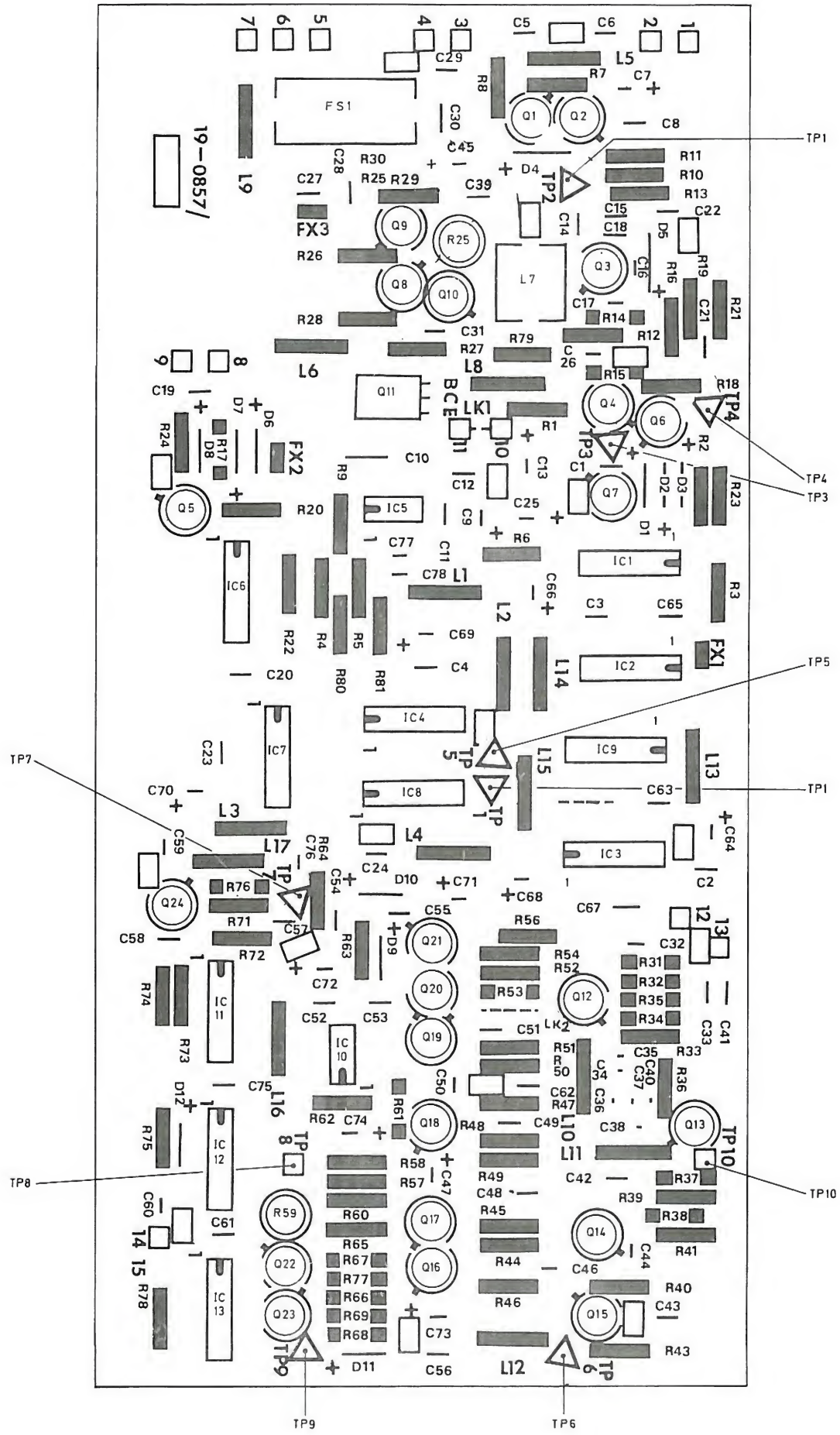
| Part No. | Description | Component Reference |
|---|---|---|
| | **Diodes** | |
| 22-1029 | Silicon, general purpose (1N4149) | D1,2,3,6,7,8, 9,10,11 |
| 22-1032 | Variable capacitance (MV1650) | D5 |
| 22-1033 | Hot carrier (HP.5082. 2811) | D12 |
| 22-1808 | Voltage reg. 5.1V (BZY-88C-5V1) | D4 |

| Part No. | Description | Component Reference |
|---|---|---|
| | **Integrated Circuits** | |
| 22-4099 | Dual J-K Bistable (74H 103) | IC1 |
| 22-4536 | Decade Counter, Schottky | IC2,3,7,8 |
| 22-4200 | Phase-Frequency Detector (MC.4044) | IC4 |
| 22-4111 | Operational Amp. (741) | IC5,10 |
| 22-4534 | Dual D-Type Bistable (74LS74) | IC6 |
| 22-4535 | Dual 4-i/p NAND gate | IC9 |
| 22-4083 | Dual NAND Schmitt Trigger (7413) | IC11 |
| 22-4505 | Quad NAND gate (74S00) | IC12,13 |

| Part No. | Description | Component Reference |
|---|---|---|
| | **Transistors** | |
| 22-6113 | Silicon, pnp, high current (ZTX.550) | Q1,2,8,9 |
| 22-6041 | Silicon, npn (BC.109) | Q10,17,18,22,23 |
| 22-6079 or 22-6017 | Silicon, npn (ZTX.313L) or (2N2369) | Q3,4,5,6,7,12,13, 14,15,16,19,20, 21,24 |
| 22-6081 | Silicon, npn 25W (MJE 520) | Q11 |

| Part No. | Description | Component Reference |
|---|---|---|
| | **Miscellaneous** | |
| 23-0003 | Fuse, quick action (See NOTE *) | FS1 |
| 23-0034 | Fuse Holder for FS1 | |
| 23-8000 | Ferrite Bead | FX1,2,3 |

*NOTE: In serial numbers 8010 to 8059 this fuse is rated at 1A (Part No. 23-0006). From serial numbers 8060 the fuse rating is 250mA (23-0003)




RACAL

| WOH 8006 | 19-0857 SHT.1 |
|---|---|
| 1 | |

Component Layout : 2nd Loop and Output Processor Assembly 19-0857

Fig. 9

÷400

PHASE COMPARATOR

LOOP INTEGRATOR

+5v(f)

PART OF 19-0856 TOP LOOP AND SAMPLER ASSY.

OSC. OUTPUT

DIVIDER I/P

TO IC 9 PIN 14 (+5V)

OSCILLATOR 19 - 21 MHz

BUFFER

REGULATOR

−7·5v(a)

(FIG. 7)

RACAL

| WOH 8006 | 19-0857 SHT 2 |
|---|---|
| 1 | |

÷400 | PHASE COMPARATOR | LOOP INTEGRATOR | ÷399

+5v(f)

FX2 | FX1

C20 100n | R20 470 | R22 4.7K | C70 10µ | C23 100n | C71 10µ | C24 100n | C69 10µ | C4 100n | C12 100n | C13 10µ | C63 100n | C64 10µ | C65 100n | R23 560 | R3 4.7K | C3 100n | C66 10µ | C67 100n | C68 10µ

L3 100µ | L4 100µ | L1 100µ | L2 100µ | L13 100µ | C2 100n | L14 100µ | L15 100µ

R6 4.7K

TO IC.9 PIN 14 (+5V)

IC6a | IC6b | IC7 ÷10 | IC8 ÷10 | IC4 | IC5 | IC1a ÷2 | IC1b ÷2 | IC2 ÷10 | IC3 ÷10

R80 470 | R4 470 | R81 470 | R5 470 | C77 100n | C78 100n | C9 10µ | R9 4.7K | C10 0.22µ | LK1 | C11 100n | C25 10µ | R1 1K | C26 1n

TP1 | TP4 | TP5

R17 6.8M | R2 6.8M | C1 100n

D6 D7 D9 | Q5 | D1 D2 D3 | Q7

C19 100n | R24 56

OSC. OUTPUT

DIVIDER I/P

PART OF 19-0856 TOP LOOP AND SAMPLER ASSY. (FIG. 7)

9a | 9b

C6 100n | C8 100n | R8 150 | Q1 | C5 100n | C7 10µ | TP2 | D4 5.1V | Q2 | R7 330 | REGULATOR | L5 100µ | L6 100µ | −7·5v(a)

R10 22K | C14 100n | L8 10µ | R13 2.2K | R12 56 | L7 1µ | C15 100n | C16 470p 5% | C17 100p | Q3 | Q4 | A79 100 | TP3 | Q6 | R11 39K | D5 | R14 18K | C18 100n | R15 470 | C21 100n | R18 1K | C22 100n | R16 1K | R19 390 | R21 180

OSCILLATOR 19 - 21 MHz | BUFFER

OSCILLATOR O/P

15 | 16

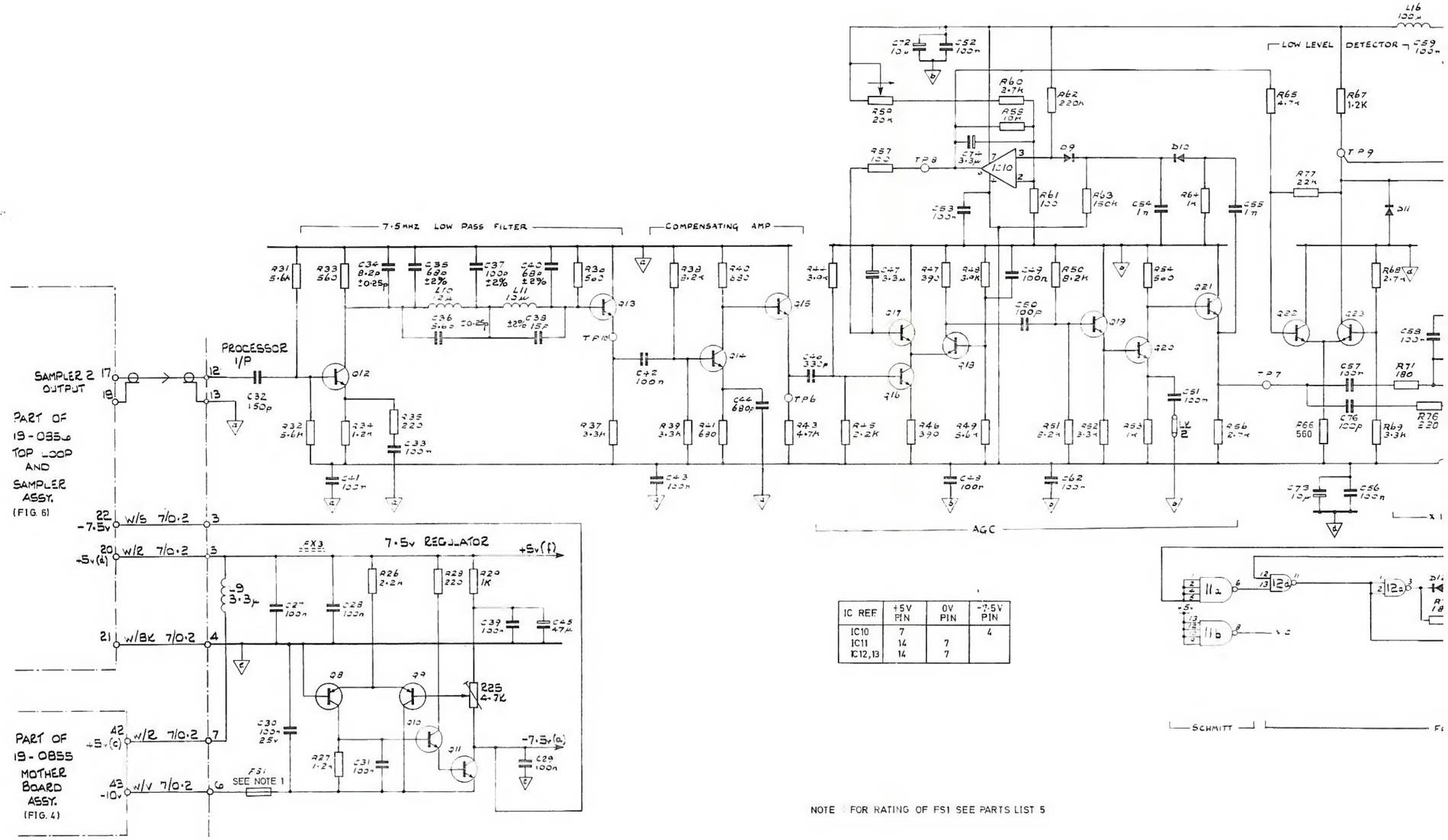
SAMPLER 2 DRIVE

PART OF 19-0856 TOP LOOP AND SAMPLER ASSY. (FIG. 6)

SCALE

1 | 8006 | 19-0857 SHT 2

**Circuit: 2nd Loop and Output Processor Assembly 19-0857 (Part 1) Fig. 10**

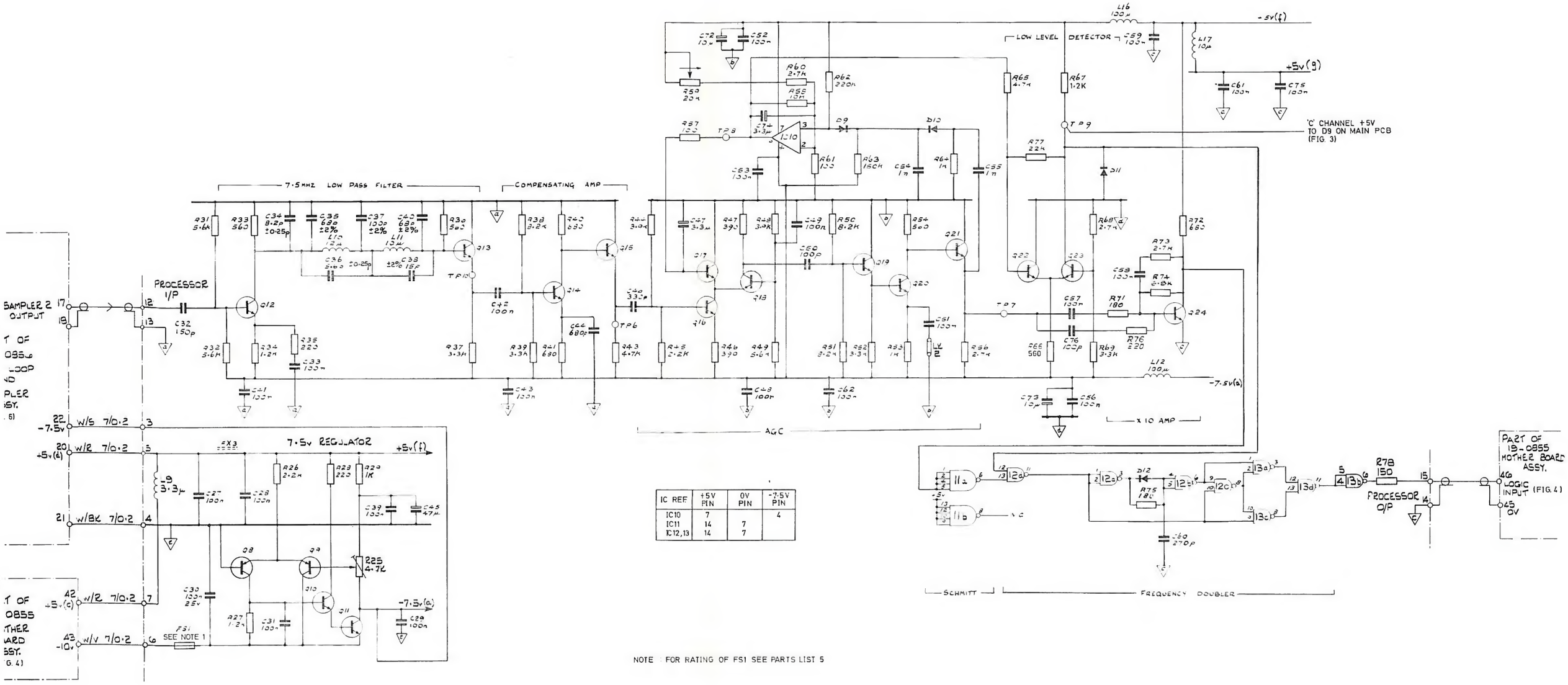



| IC REF | +5V PIN | 0V PIN | -7.5V PIN |
|---|---|---|---|
| IC10 | 7 | | 4 |
| IC11 | 14 | 7 | |
| IC12,13 | 14 | 7 | |

NOTE : FOR RATING OF FS1 SEE PARTS LIST 5

RACAL

| WOH8006 | 19-0857 SHT. 3 |
|---|---|
| 1A | |




| IC REF | +5V PIN | 0V PIN | -7·5V PIN |
|---|---|---|---|
| IC10 | 7 | | 4 |
| IC11 | 14 | 7 | |
| IC12,13 | 14 | 7 | |

NOTE : FOR RATING OF FS1 SEE PARTS LIST 5

8006 | 19-0857 SHT. 3

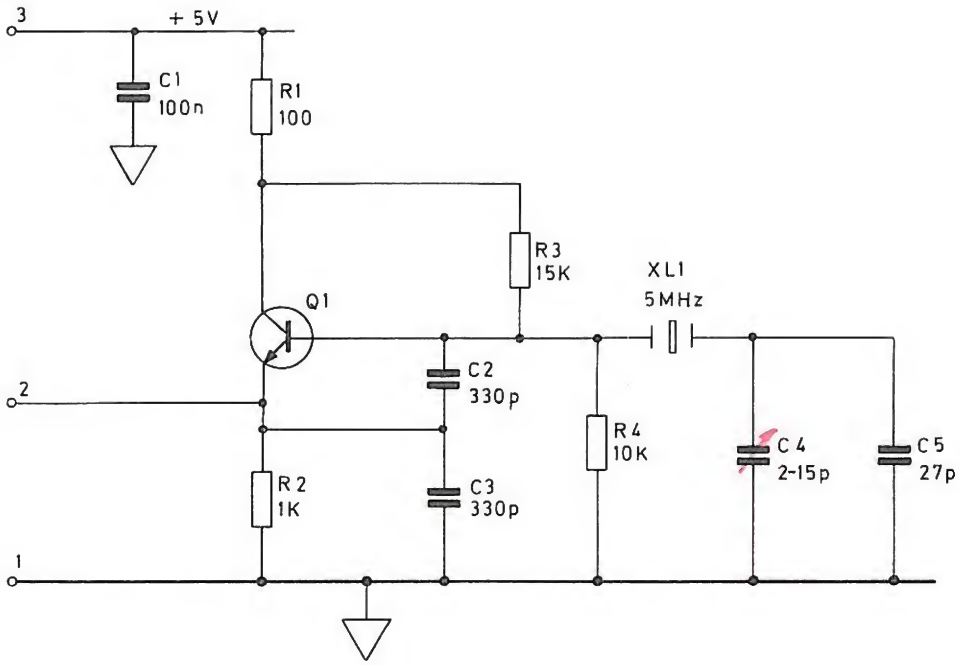
Circuit: 2nd Loop & Output Processor Assembly 19-0857 (Part 2) Fig. 11

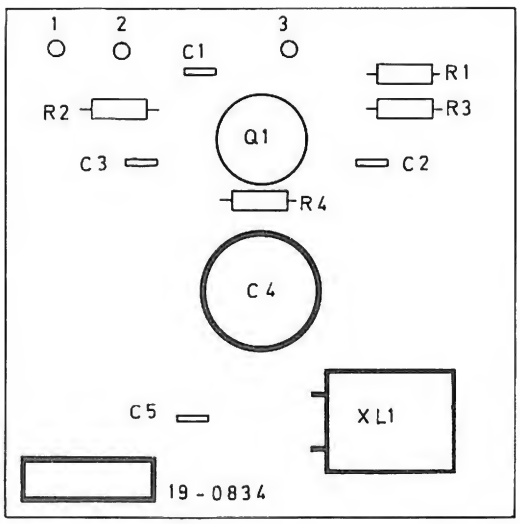
## PARTS LIST FOR FIG. 12

## 5 MHz CRYSTAL OSCILLATOR ASSEMBLY (19-0834)

## (OPTION 04C)

| Part No. | Description | Rat | Tol % | Value | Component Reference |
|---|---|---|---|---|---|
| | Resistors | W | | Ω | |
| 20-2101 | Carbon Film | $\frac{1}{4}$ | 5 | 100 | R1 |
| 20-2102 | Carbon Film | $\frac{1}{4}$ | 5 | 1k | R2 |
| 20-2103 | Carbon Film | $\frac{1}{4}$ | 5 | 10k | R4 |
| 20-2153 | Carbon Film | $\frac{1}{4}$ | 5 | 15k | R3 |
| | Capacitors | V | | F | |
| 21-1616 | Ceramic | 12 | 20 | 100n | C1 |
| 21-2621 | Silver Mica | 125 | 5 | 27p | C5 |
| 21-2631 | Silver Mica | 125 | 5 | 330p | C2,3 |
| 21-6030 | Trimmer | | | 2-15p | C4 |
| | Transistors | | | | |
| 22-6017 | Silicon NPN (2N2369) | | | | Q1 |
| | Crystal | | | | |
| 17-2087 | Crystal Assembly, 5 MHz | | | | XL1 |




| WOH 8006 | 19-0834 |
|---|---|
| 1 | |

Circuit And Layout:
5MHz Oscillator PCB 19-0834

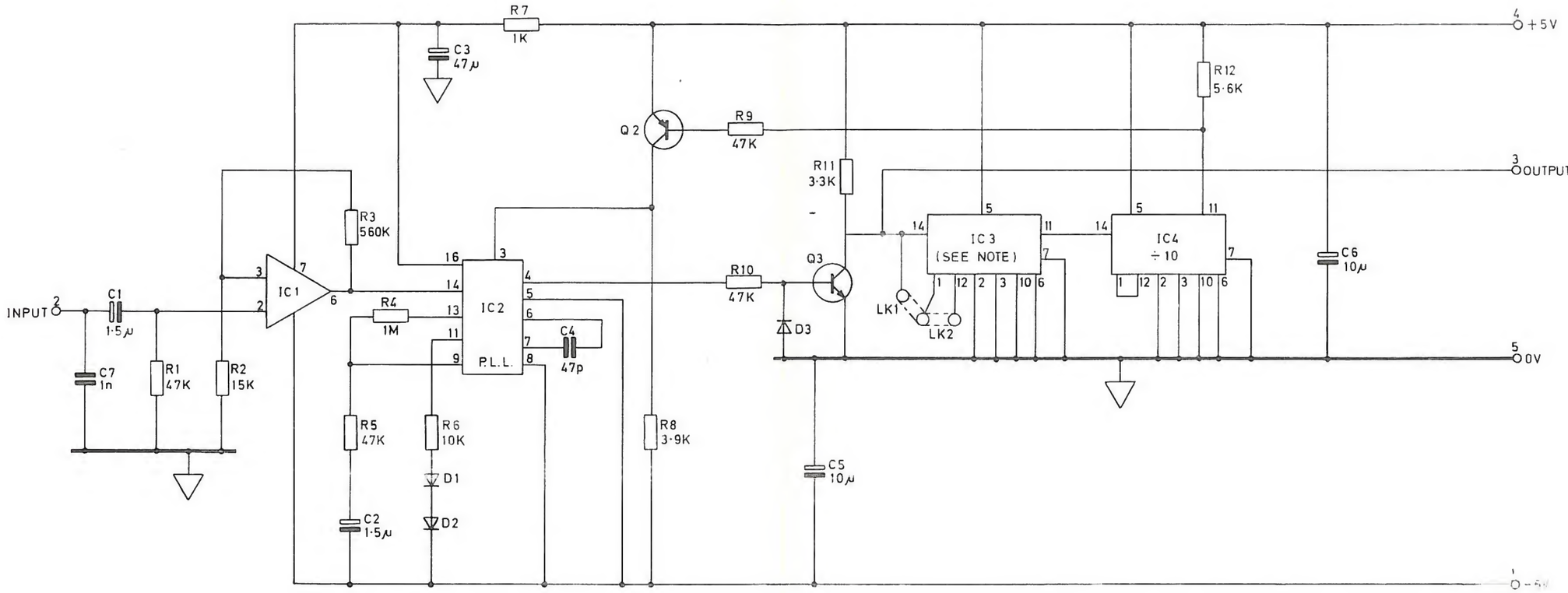
Fig. 12

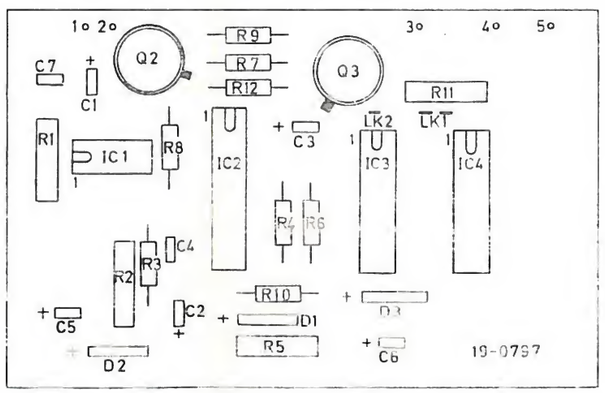
## PARTS LIST FOR FIG. 13

## LF FREQUENCY MULTIPLIER ASSEMBLY 19-0797

(OPTION)

| Part No. | Description | Rat | Tol % | Value | Component Reference |
|---|---|---|---|---|---|
| | Resistors | W | | Ω | |
| 20-2102 | Carbon Film | ¼ | 5 | 1k | R7 |
| 20-2103 | Carbon Film | ¼ | 5 | 10k | R6 |
| 20-2105 | Carbon Film | ¼ | 5 | 1M | R4 |
| 20-2153 | Carbon Film | ¼ | 5 | 15k | R2 |
| 20-2332 | Carbon Film | ¼ | 5 | 3.3k | R11 |
| 20-2392 | Carbon Film | ¼ | 5 | 3.9k | R8 |
| 20-2473 | Carbon Film | ¼ | 5 | 47k | R1,5,9,10 |
| 20-2562 | Carbon Film | ¼ | 5 | 5.6k | R12 |
| 20-2564 | Carbon Film | ¼ | 5 | 560k | R3 |
| | Capacitors | | | F | |
| 21-1002 | Tantalum | 20V | 20 | 10µ | C5,6 |
| 21-1029 | Tantalum | 35V | 20 | 1.5µ | C1,2 |
| 21-1038 | Tantalum | 6.3V | 20 | 47µ | C3 |
| 21-1516 | Ceramic | 500V | 10 | 47p | C4 |
| 21-1532 | Ceramic | 500V | 20 | 1n | C7 |
| | Diodes | | | | |
| 22-1029 | Silicon (1N4149) | | | | D1,2,3 |
| | Integrated Circuits | | | | |
| 22-4111 | Operational Amplifier (741C) | | | | IC1 |
| 22-4536 | Decade Counter, low power (74LS90) | | | | IC3,4 |
| 22-4703 | CMOS Phase-Locked Loop (CD4046AE) | | | | IC2 |
| | Transistors | | | | |
| 22-6017 | Silicon NPN (2N2369) | | | | Q3 |
| 22-6113 | Silicon PNP (ZTX 550) | | | | Q2 |




NOTE : FOR USE IN 9918 AND 9921
FIT LINK LK 2
DO NOT FIT LINK LK1

| WOH 8006 | 19-0797 |
|---|---|
| 1 | |

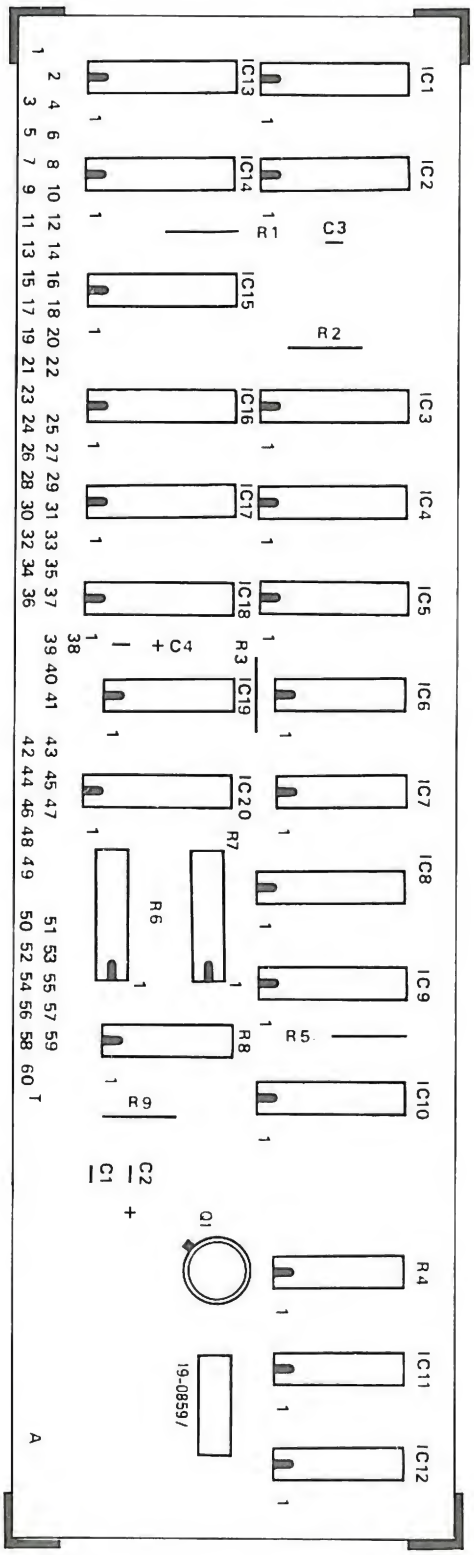
Circuit and Layout :
LF Multiplier Assembly

Fig.13

## PARTS LIST OPTION FIG. 15

## REMOTE AND BCD OPTION ASSEMBLY 19-0859

| Part No. | Description | Rat. | Tol. | Value | Component Reference |
|---|---|---|---|---|---|
| | Resistors | W | % | Ω | |
| 20-2181 | Carbon Film | ¼ | 5 | 180 | R1, 3, 9 |
| 20-2332 | Carbon Film | ¼ | 5 | 3.3k | R2 |
| 20-2123 | Carbon Film | ¼ | 5 | 12k | R5 |
| 20-5507 | DIL Array (13) | | | 3.3k | R4 |
| 20-5508 | DIL Array (7) | | | 1k | R6, 7, 8 |
| | Capacitors | V | % | F | |
| 21-1616 | Ceramic | 12 | -20 +80 | 100n | C1, 3 |
| 21-1038 | Tantalum | 6.3 | 20 | 47µ | C2 |
| 21-1041 | Tantalum | 35 | 20 | 1µ | C4 |
| | Integrated Circuits | | | | |
| 22-4704 | CMOS 8-bit shift reg. (CD4015) | | | | IC1, 2, 3, 4 |
| 22-4705 | CMOS Quad D-Type Bistable (340175PC) | | | | IC5 |
| 22-4549 | Triple 3 i/p NORgate (74LS27) | | | | IC6 |
| 22-4534 | Schottky dual D-Type Bistable (74LS74) | | | | IC7, 19 |
| 22-4719 | CMOS Hex Inverter (4049) | | | | IC8, 13, 14, 15, 16, 17, 18 |
| 22-4216 | Transistor Array, npn (CA.3083) | | | | IC9, 10 |
| 22-4546 | 2 i/p Schottky NAND gate o/c (74LS03) | | | | IC11 |
| 22-4548 | Triple 3 i/p NAND gate o/c (7412) | | | | IC12 |
| 22-4717 | CMOS Hex non-inverting buffer (4050) | | | | IC20 |
| | Transistors | | | | |
| 22-6079 | Silicon, npn (ZTX313L) | | | | Q1 |

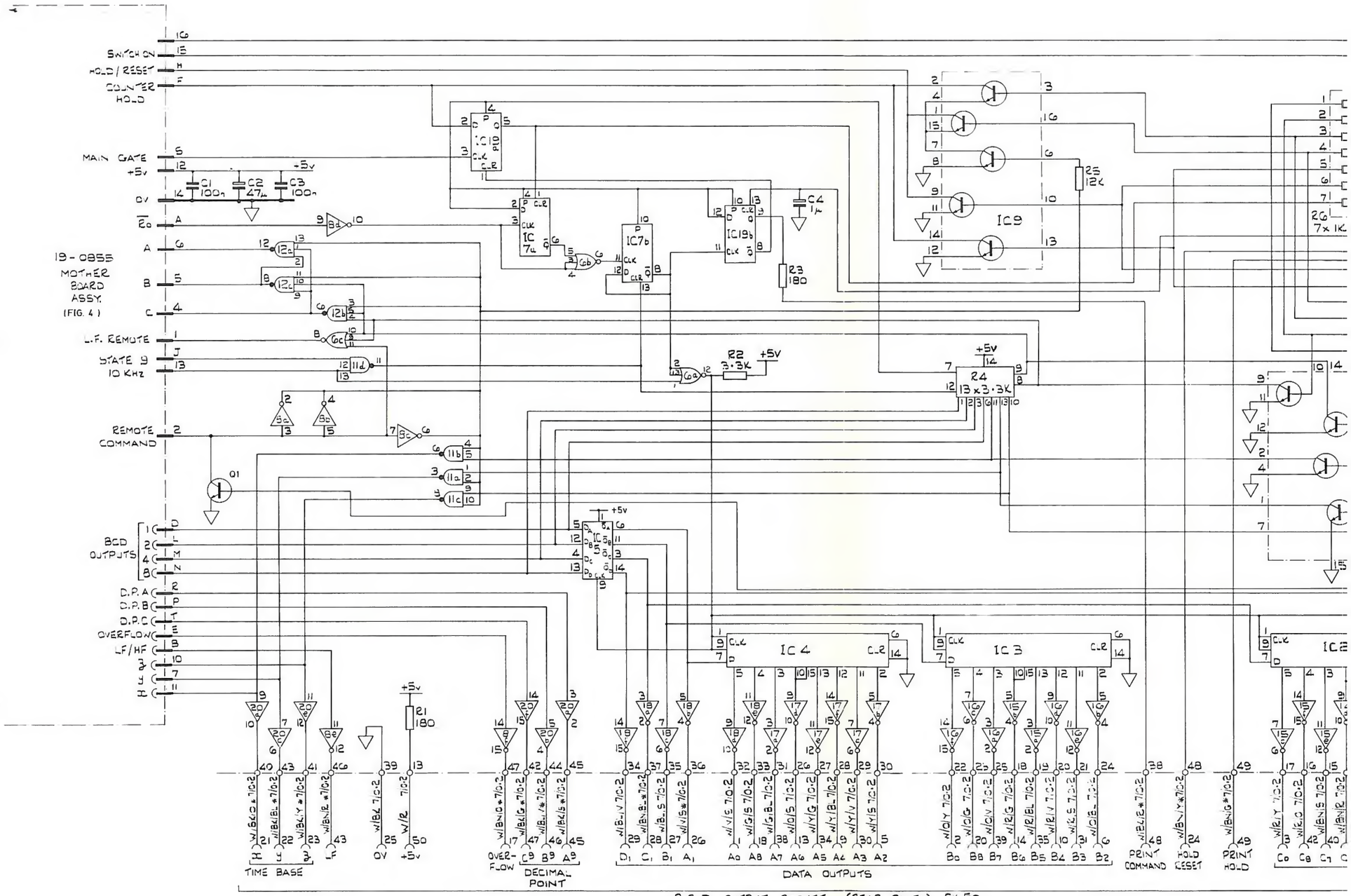



RACAL

| WOH 8006 | 19-0859 SHT1 |
|---|---|
| 1 | 2 |

Component Layout: Remote Control & BCD Output Assembly 19-0859

Fig.14




B.C.D. OUTPUT SOCKET (REAR PANEL) SK 50

| REFERENCE | PART No. | 0V | +5v | TYP. TYPE No |
|---|---|---|---|---|
| IC9.10 | 22-4216 | 5 | | 3083 |
| IC7.19 | 22-4534 | 7 | 14 | 74LS74 |
| IC11 | 22-4546 | 7 | 14 | 74LS03 |
| IC12 | 22-4548 | 7 | 14 | 74LS12 |
| IC6 | 22-4549 | 7 | 14 | 74LS27 |
| IC1-4 | 22-4704 | 8 | 16 | 14015 |
| IC5 | 22-4705 | 8 | 16 | 74C175 |
| IC20 | 22-4717 | 8 | 1 | 4050 |
| IC8,13-18 | 22-4719 | 8 | 1 | 4049 |

RACAL

| WOH 8006 | 19-0859 SHT. 2 |
|---|---|
| 1 2 | |

| REFERENCE | PART No. | 0V | +5v | TYP. TYPE No |
|---|---|---|---|---|
| IC9.10 | 22-4216 | 5 | | 3083 |
| IC7.19 | 22-4534 | 7 | 14 | 74LS74 |
| IC11 | 22-4546 | 7 | 14 | 74LS03 |
| IC12 | 22-4548 | 7 | 14 | 74LS12 |
| IC6 | 22-4545 | 7 | 14 | 74LS27 |
| IC1-4 | 22-4704 | 8 | 16 | 14015 |
| IC5 | 22-4705 | 8 | 16 | 74C175 |
| IC20 | 22-4717 | 8 | 1 | 4050 |
| IC8,13-18 | 22-4719 | 8 | 1 | 4049 |

Circuit : Remote and BCD
Option Assembly 19-0859 Fig. 15